A Novel Resonant LLC Soft-Switching Inverting-Buck Converter

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***Abstract*— a new soft-switching resonant inverting-buck converter with high efficiency is presented. The proposed converter steps down and inverts the input voltage. The zero-current-switching (ZCS) technique is employed to reduce switching losses and Electromagnetic Interferences (EMI). An LLC resonant network is utilized to provide soft-switching conditions for all semiconductor devices. Experimental results verify the integrity of the proposed converter operation and the presented theoretical analysis.**

***Keywords* — inverting- buck converter; soft-switching; resonant power conversions; ZCS; power supply.**

I. INTRODUCTION

Switching converters have been widely employed for DC–DC power conversion because the converter operating frequency is considerably increased and consequently the converter size and weight are reduced. Operational amplifiers (OP-AMP), dynamic read-only memories (RAM), localized micro-processors, data acquisition systems and telecommunication modules are the general devices/systems wherein a regulated supply with negative voltage is required. In these applications, it is essential to reduce the converter size and loss, and isolation is not required.

Soft-switching techniques are developed to reduce switching losses and electromagnetic interference (EMI). At soft-switching condition, switching frequency can be increased to enhance the converter power density. This condition is commonly attained by zero-voltage switching (ZVS) and/or zero-current switching (ZCS) [1]–[20].

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To provide a regulated negative voltage, the PWM buck-boost converter, and switched capacitor converters (SCCs) are employed classically. Quasi-resonant buck-boost converter is a soft-switching counterpart of the PWM buck-boost converter in which a high-frequency resonant tank is utilized to reduce switching losses. The main advantage of this technique is its less additional elements. However, two inductors are required where the main inductor of parent converter is still a relatively bulky component. Moreover, the voltage stress of switch is higher than that of the PWM counterpart [2]–[5]. SCCs are attractive for chip design purposes because no magnetic component is utilized. A major drawback is the current spikes produced by charging /discharging of the circuit capacitors via only parasitic resistors of the switches. Very low power handling and high EMI are consequences of this kind of operation [6], [7]. Resonant SCCs (RSCs) are SCC alternatives in which the switches current is controlled by placing a small inductor in series with the switching capacitors [6]–[13]. However, not only the converter voltage gain is not adjustable in RSCs [13], but also it varies against load changing [9]. To provide a fractional voltage gain, many diodes and capacitors ought to be used, which result in an increase of the converter cost, volume and conduction losses [8], [9].

Resonant converters are a family of soft-switching converters, in which energy is transferred through a high frequency resonant tank and switching is performed at zero-crossing instants of current and/or voltage. The main advantage of resonant converters is that the size of passive components is reduced greatly [1], [6]–[18]. In series-resonant converter (SRC), the converter passive components include only a high-frequency resonant tank and a filtering capacitor at the output [1], [14], [15]. The significant limitation of conventional resonant converters is that the source and load do not possess common ground between input and output terminals. Hence, these converters are mostly viewed for isolated purposes. Employing a transformer to create a common ground seems to be unreasonable for the aforementioned applications.

This paper presents a new resonant soft-switching step-down converter with inverted output voltage polarity. The passive components include only a high frequency resonant LLC tank and a filtering capacitor at the output. However, the proposed converter possesses common ground between input and output terminals and hence is suitable for non-isolated applications. All semiconductor devices operate under soft-switching condition at turn-on and turn-off switching instants, independent of the load current and operating voltages. Unlike RSCs, voltage gain is adjustable and less number of elements is employed. Comparing with [19]-[20], one small resonant inductor is added (LLC tank); however, the number of diodes are decreased from 4 in [19] to 1 in this paper, which results in less conduction losses and lower price. Moreover, the added inductor inhibits creation of spiky current produced in the conventional bridge arms due to the severe reverse recovery problem of the switches anti-parallel diodes. The converter can be designed to limit output power and is automatically shut down at output short circuited. Experimental results from a 10W/100 kHz prototype verify the integrity of operation and presented theoretical analysis.

II. ANALYSIS OF PROPOSED BUCK CONVERTOR

Fig. 1 illustrates the topology of proposed inverting-buck converter which is constructed by two switches Q_1, Q_2, a resonant LLC network (L_{r1}, L_{r2}, and C_r), the rectifying diode D_r, and the output filtering capacitor C. The corresponding equivalent circuits and steady-state waveforms are shown in Figs. 2 and 3.

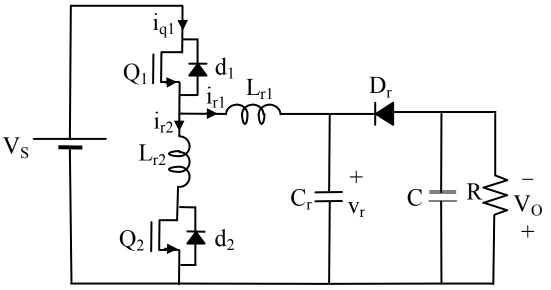


Fig. 1 Proposed buck converter topology

Following quantities are defined.

$$L_r = L_{r1} + L_{r2} \ , \ \alpha = \frac{L_{r1}}{L_r} \tag{1}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \ , \ f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \ , \ r = \frac{R}{Z_r} \ , \ A = \frac{V_o}{V_s} \tag{3}$$

$$V_r(t) = \frac{v_r(t)}{V_s} \ , \ I_{r1}(t) = \frac{i_{r1}(t)}{V_s/Z_r} \tag{4}$$

For simplicity it is assumed all the circuit elements are ideal and the output capacitor is large enough so that the output voltage is constant during one switching cycle. The initial currents of all inductors are zero and the initial voltage of the resonant capacitor C_r is $V_r=V_O$. The circuit has five operating modes as follows.

Mode I (t_0-t_1): At t_0 Q_1 is turned on. Since the initial currents of both inductors are zero, according to KCL, Q_1 turn-on is under the ZCS conditions. The resonant inductor L_{r2} inhibits creation of spiky current at the turn-on instant of Q_1 which is created in the conventional bridge structure due to the severe reverse-recovery of the anti-parallel diode of Q_2 and its output capacitance. After one half sinusoidal- cycle the current of Q_1 reaches zero and hence this switch is turned off at ZCS. During this mode C_r has been charged up to $2V_S$-V_O.

$$I_{r1}(t) = \frac{(1-A)}{\sqrt{\alpha}} \sin\left(\frac{\omega_r}{\sqrt{\alpha}}(t-t_0)\right) \tag{5}$$

$$V_r(t)=1-(1-A)\cos\left(\frac{\omega_r}{\sqrt{\alpha}}(t-t_0)\right) \tag{6}$$

$$t_1-t_0=\frac{\sqrt{\alpha}T_r}{2} \tag{7}$$

$$V_r(t_1)=(2-A) \tag{8}$$

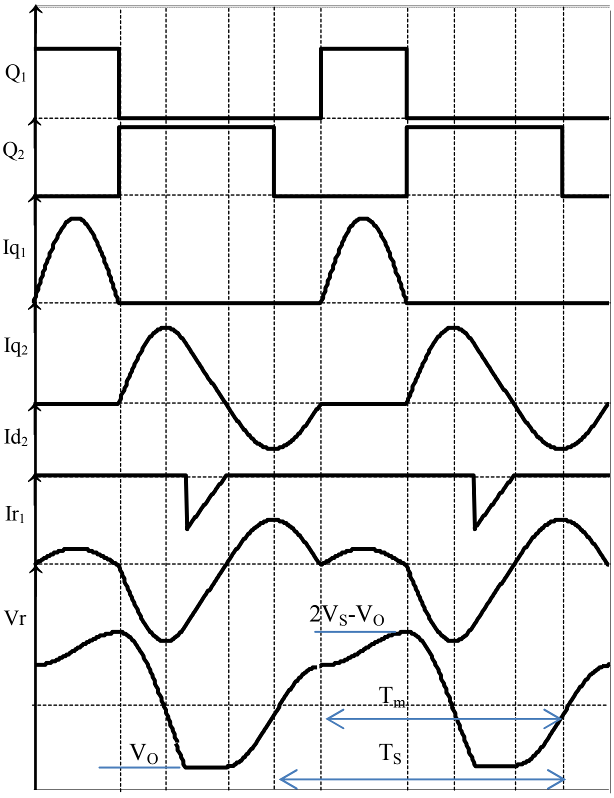


Fig. 2 Steady-state key waveforms

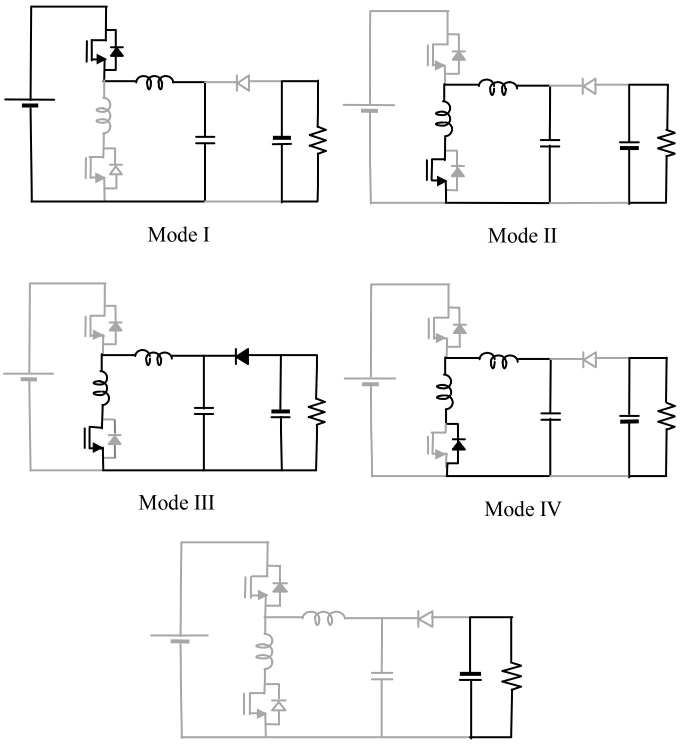
Mode *II* (*t_1-t_2*): Q_2 is turned on at t_1 under the ZCS conditions. The voltage of C_r starts reversing through a resonance with L_{r1} and L_{r2} until at t_2 the resonance voltage v_r reaches $-V_O$.

$$I_{r1}(t)=(A-2)\sin(\omega_r(t-t_1)) \tag{9}$$

$$V_r(t)=(2-A)\cos(\omega_r(t-t_1)) \tag{10}$$

$$t_2-t_1=\frac{1}{\omega_r}\left[\pi-\cos^{-1}\frac{A}{2-A}\right] \tag{11}$$

$$I_r(t_2)=-2\sqrt{1-A} \tag{12}$$



Mode I

Mode II

Mode III

Mode IV

Mode V

Fig. 3 Equivalent circuits of the proposed buck converter

Mode III (*t_2-t_3*): At t_2, the diode D_r is forward biased and clamps the voltage of C_r at $-V_O$. The stored magnetic energy in L_{r1} and L_{r2} is delivered to the output via this diode. By demagnetizing L_{r1} and L_{r2} at t_2, the switch Q_2 and the diode D_r both turned off at ZCS.

$$I_{r1}(t)=I_{r1}(t_2)+A\omega_r(t_3-t_2) \tag{13}$$

$$V_r(t)=-A \tag{14}$$

$$t_3-t_2=\frac{2\sqrt{1-A}}{A\omega_r} \tag{15}$$

$$I_r(t_3)=0 \tag{16}$$

Mode IV (*t_3-t_4*): In this period the anti-parallel diode of Q_2 is forward biased at ZCS and thus the voltage polarity of C_r reverses via a resonance with L_{r1} and L_{r2}. The gate signal of Q_2 can be reset at any instant during this interval.

$$I_{r1}(t)=A\sin(\omega_r(t-t_1)) \tag{17}$$

$$V_r(t) = -A\cos(\omega_r(t-t_1)) \tag{18}$$

$$t_4 - t_3 = \frac{T_r}{2} \tag{19}$$

$$V_r(t_4) = V_o \tag{20}$$

Mode V (t_4-t_5): In this mode, Q_1 and Q_2 are OFF and the load is supplied by the output capacitor. Duration of this interval is determined by the controller so that proper voltage regulation is attained (dead-time control).

III. VOLTAGE GAIN

At steady state, the converter voltage gain can be calculated by satisfying the energy conservation principle in one Switching cycle as (21). By substituting (5) into (21) and simplifying, (22) is obtained in which $f_s=1/T_s$ is the switching frequency.

$$\int_{t_0}^{t_1} V_s i_{r1} dt = \frac{V_o^{2}}{R} T_s \tag{21}$$

$$S = \frac{r}{\pi}.\frac{f_s}{f_r} = \frac{A^2}{1-A} \tag{22}$$

In absence of dead-time (Mode V), the converter operates at its maximum power handling capability, where the switching frequency is also at maximum. Maximum voltage gain $A=A_m$ Is also attained at this situation. The interval from t_0 to t_4 is defined as T_m. By using (7), (11), (15), (19) following relation is obtained.

$$\frac{T_m}{T_r} = 1 + \frac{\sqrt{\alpha}}{2} + \frac{1}{\pi}\left[\frac{\sqrt{1-A}}{A} - \frac{1}{2}\cos^{-1}\frac{A}{2-A}\right] \tag{23}$$

By substituting $f_s = T_m^{-1}$ in (22), (24) is obtained, wherein in fact, A_m is a function of r. This equation is required for converter design. A_m against r/π is sketched in Fig. 4.

$$r = \frac{A_m^{\ 2}}{1-A_m}\left[\pi + \frac{\pi\sqrt{\alpha}}{2} + \frac{\sqrt{1-A_m}}{A_m} - \frac{1}{2}\cos^{-1}\frac{A_m}{2-A_m}\right] \tag{24}$$

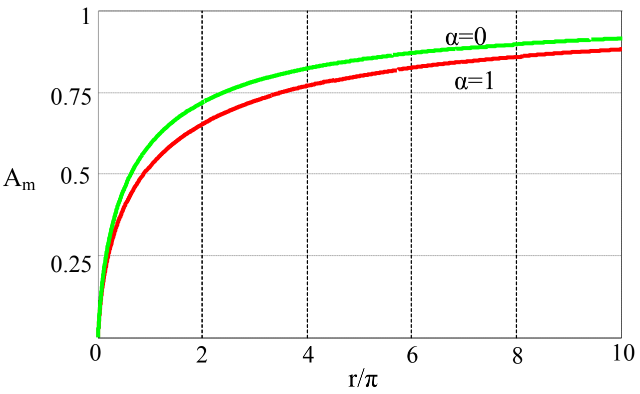


Fig. 4 Maximum attainable voltage gain against r/π

At output short circuited, A is zero and thus according to (23) T_m goes infinity. Since T_m is the shortest switching period, power transferring is automatically stopped when the output is short-circuited (self short-circuit protection).

IV. DESIGN PROCEDURE – AN EXAMPLE

The parameter α can be used as one degree of freedom for optimizing the converter. For a given value of α, the converter design is performed as follows.

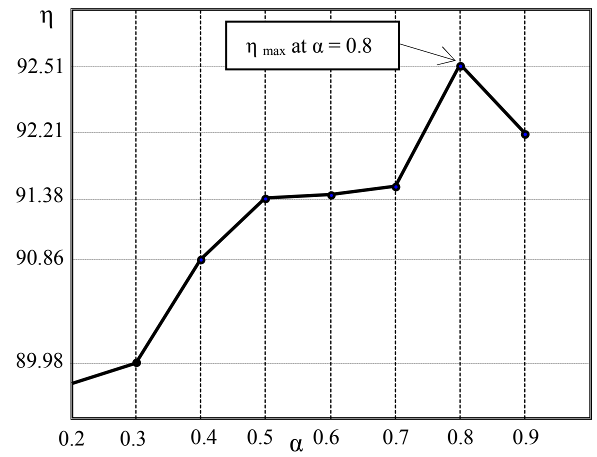


Fig. 5 Maximum attainable efficiency against α

The maximum attainable voltage gain is obtained as $A_m=V_O/V_{S\ min}$. By substituting A_m in (24), the normalized load, r, is calculated. Then according to (3), the resonant tank characteristics impedance is obtained by $Z_r=P_{out\ max}/r$. The resonant tank characteristics angular frequency ω_r determines switching frequency and should be ascertained by considering the technology of the employed switches.

Example: Consider a 10W prototype converter for V_s=48V±10% to Vo=36V±1% with 10% overdesign and resonant frequency f_r=100KHz.

Solution: The converter is designed by employing the aforementioned procedure for several values of α. Here, the parameter α is used to optimize the converter efficiency. Variations of the converter efficiency versus α are shown in Fig. 5. This curve is obtained by simulating the converter with OrCAD PSpice software.

According to Fig. 5, the efficiency is maximum for α=0.8. Then the converter elements are calculated as L_{r1}=14.03µH, L_{r2}=3.50 µH, C_r=144nF and C=33µF.

V. EXPERIMENTAL RESULTS

The employed switches are Q_1=IRF640, Q_2=IRF540, and D_r=BYT56. Both inductor cores are ferrite, and the resonant capacitor is MKP type (metalized polyethylene). A guard-time about 400ns exists between Q_2 turn-off and Q_1 turn-on. For P_{out}=10W, the practical results of the designed prototype are shown in Fig. 6. According to this figure, soft-switching conditions are attained for both switches at both turn-on and turn-off switching instants. The ringing wave of voltage switches appeared at turn-off instants are due to the switches output capacitances which oscillate with the tank inductances.

VI. CONCLUSIONS

A new LLC resonant step-down converter with inverted voltage polarity is presented. The proposed converter can be applied for producing negative voltage from a positive voltage. All semiconductor devices operate at soft-switching conditions which results in high efficiency and low EMI. Experimental results confirm the integrity of the theoretical analysis.

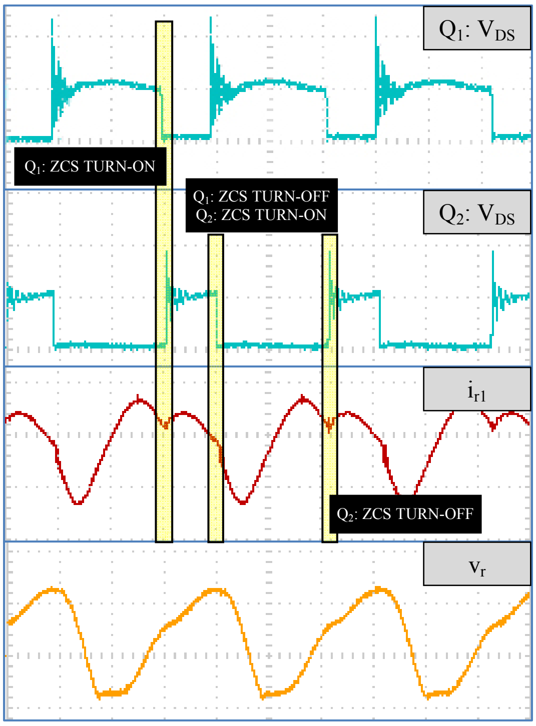


Fig. 6 Practical Results, respectively from the top: V_{DS} of Q_1 (50V/div), V_{DS} of Q_2 (50V/div), I_{r1} (200mA/div), and V_r (50V/div). Time scale=5µs/div.

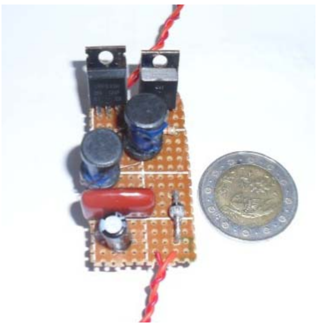


Fig. 7 Implemented converter

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