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A Low Power 2.5Gb/s CMOS Optoelectronic Amplifier

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Abstract: In this paper, a low power 2.5Gb/s CMOS optoelectronic amplifier is designed using a standard 0.18μm CMOS technolog. Design consists of a transimpedance amplifier (TIA) and 4 stages limiting amplifier (LA). In this design TIA is based on push-pull inverter topology with voltage-current active feedback and LA designed based on basic common-source differential pair topology with inductive peaking technique for bandwidth extension. Simulation were performed using TSMC 0.18μm CMOS technology in HSPICE software. The resuls shows the following performance: the TIA has a 53dBΩ transimpedance gain and 1.8GHz bandwidth, the LA has a 38dB gain and 2GHz bandwidth. The differential voltage swing at the LA output is 640mV and power consumption TIA and LA from a 1.5V power supply are 794μW and 4mW respectively. The results indicate this design is suitable as optoelectronic amplifier for a 2.5Gb/s communications over fiber optic.

Index Terms: optical communications, transimpedance amplifier, limiting amplifier, inductive peaking, low power

I. INTRODUCTION

The exponential growth of the internet and multimedia communications has greatly increased the demand for a high speed communication systems, leading to extensive work on high speed device and circuit design. The composed circuit in the optoelectronic amplifier are required to have high frequency operation, low cost and low power consumption. CMOS technology is a preferable candidate to achieve a low cost solution due to its high integration characteristic. However, its parasitics limit the performance of broadband amplifiers. In optical communication systems an optical receiver is one of the key components, where it acts as the interface between the electronis and the optics. The overall purpose of the circuit is to convert an optical signal, which may have been attenuated and corrupted by noise and dispersion in the optical link, into a clean, high level electronic signal that can be used as an input to logic circuitry or to regenerate the optical signal.

Fig.1 shows a block diagram of the typical optical receiver for optical communication systems.It consists of a photodiode, transimpedance amplifier (TIA), limiting amplifier (LA), clock and data recovery (CDR) and a demultiplexer(DMUX). TIA which convert and amplifies the photodiode current into a voltage, requires high gain, wide bandwidth, low noise and low input impedance with low power consumption. Since the TIA output swing may not be large enough to provide logical levels, a high gain amplifier that called LA must follow the TIA. LA provide both a high voltage gain and large output swing. Subsequence block that connected to th LA is CDR circuitry. The purpose of the CDR block is to extract the clock timing from the incoming data, while also retiming the data and reducing its jitter. Finally by using a DMUX data convert of serial to parallel and reproduce the original parallel channels[1]. In this paper, a suitable design is proposed for optoelectronic amplifier that consisting of the TIA and LA blocks.

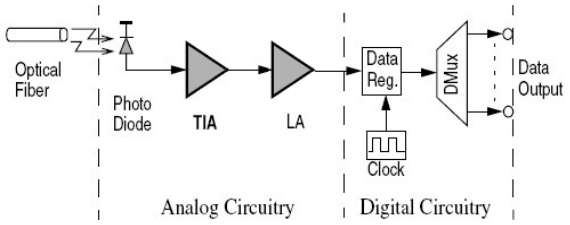


Figure. 1: Block diagram of optical receiver

II. TIA

TIA is one of the most critical block in an optical receiver. The design of TIAs entails many trade-off between gain, bandwidth, noise and power consumption. The TIA bandwidth is typically chosen to be equal to 0.65 times the bit rate, a reasonable compromise between the total integrated noise and the intersymbol interference (ISI) resulting from limited bandwidth. Two limiting factors of the design of the TIA are the input capacitance introduced by the photodiode and the resistor closing the negative feedback link around the TIA. Fig.2 shows a generalized schematic of a TIA used in an optic system[1,6].

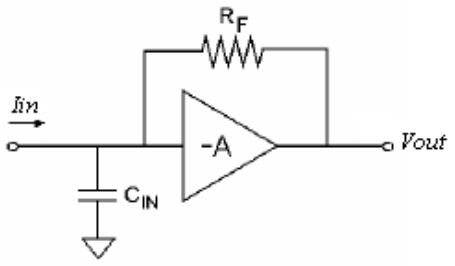


Fig. 2: Typical TIA Configuration

Careful selection of the open-loop voltage amplifier topology is necessary for maximizing the Transimpedance-Bandwidth product. We compared several open-loop topologies before selecting the Push-Pull inverter topology. This configuration looks like a digital inverter, but the transistor gates are biased so that the transistors are in saturation. At this bias point the inverter is in its high-gain region. An additional advantage to this topology is the self-biasing nature of the circuit [2, 3]. The proposed TIA is shown in Fig. 3.

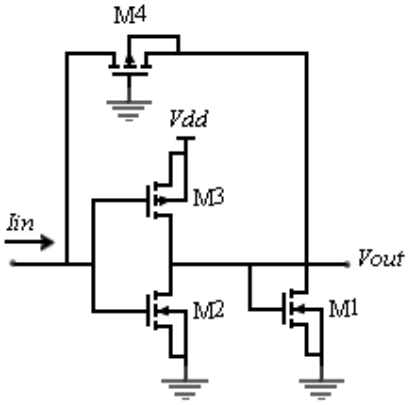


Fig. 3: proposed design for TIA

The circuit consists of four transistor. Transistors M2 and M3 are used as push-pull inverter, transistor M1 operates as a diode NMOS at the output of circuit to reduce the gain of the amplifier and extend its bandwidth. The voltage gain of the amplifier is given by:

$$A = \frac{g_{m3} + g_{m2}}{g_{m1}} \tag{1}$$

Where g_m is the transconductance transistors. M4 act as a feedback resistance. In order to reduce the input-referred noise current and avoid process variation problems, active feedback is used instead of resistor feedback. We have used a PMOS device in its linear region for the feedback resistance [4].

To maximize the voltage swing at the output, it is desirable to set Vin = Vout = Vdd/2 at DC. This implies that:

$$V_{GS3} = V_{GS2} = V_{GS1} \tag{2}$$

and

$$W_3 = \frac{\mu_n}{\mu_p}(W_2 + W_1) \tag{3}$$

Where μ is the mobility and W_i is the width of a CMOS transistor. It was found that a large range of feedback resistances could be achieved with limited variations in the drain and source capacitances of M4. Under the condition that the feedback impedance is independent of $C_{GS2,3}$, the optimal input capacitance necessary to minimize noise is the same as that of the photodiode C_{diode}. For stability, the dominant pole at the input node should be at half or less the frequency of the second pole at the output node [4, 6]. The dominant pole can be shown to be situated at [5]:

$$P_1 = \frac{1 + A}{(C_{diode} + C_{in})R_f} \tag{4}$$

Where R_f is the value of the feedback resistance due to M4, while A is the open loop gain of the amplifier in V/V. The second pole can be shown to be at [3,5]:

$$P_2 = \frac{1}{C_{out}R_{out}} \tag{5}$$

The total output capacitance C_{out} is dependent on M1, M2, and M3, and the output resistance R_{out} is dominated by the g_m of M1. The second pole can be adjusted through W_2/W_1 while keeping $W_2 + W_1$ fixed. This leaves W_4 as an extra degree of freedom, which can be used to maximize the bandwidth until the TIA reaches the limit of stability.

III. LA

The goal of the LA is to provide an output with a fixed voltage swing independent of the signal current at the TIA input. Design of a LA with a high speed, a high gain, and a wide dynamic range is a basic task for the realization of high speed data systems. The LA relies on the cascade of limiting differential amplifier pairs with enough bandwidth and a relatively linear phase response so as to amplify the signal with negligible ISI [1, 2].

In this design, taking into account the TIA performance the LA is realized by means of four gain stages. The block diagram of the LA presented in this paper is shown in Fig. 4.

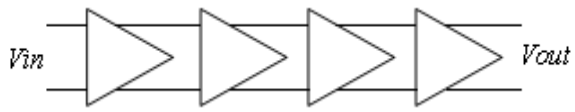


Fig. 4: System block of LA

In this design LA employ scaling technique, and scaling factor α =1.2 is applied to the widths of all MOS transistors and current sources of the driving gain stage such that the transistor size in the driven stage are α times smaller than those in the driving stage [9]. Assuming that each gain stage has one dominant pole and

it is strongly dependent on the total load capacitance of the stage consisting of the stage output capacitance C_o, the wiring capacitance C_w and the input capacitance C_i of the next stage, the bandwidth extension factor *k* of the nth gain stage can be defined as [2]:

$$k = \frac{C_{o1} + C_{i1} + C_w}{(1/\alpha)^{n-1}(C_{o1} + C_{i1}) + C_w} \quad (6)$$

As shown, a significant bandwidth extention can be achieved for all stages.

The four amplifying cell have the same circuit topology as shown in Fig. 5.

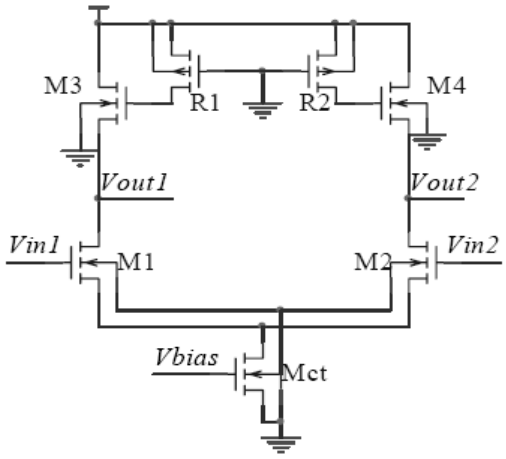


Fig. 5. Circuit topology of an individual gain stage

Each stage is a basic common-source differential. In order to alleviate the bandwidth degradation caused by the parasitic capasitances, active inductor were implementd for bandwidth enhancement. The idea is to allow the capacitance that limits the bandwidth to resonate with an inductor, thereby improving the speed. The resonance must of course occur with minimal peaking and overshoot so as to provide a well-behaved response to random data [1]. In this design, active inductor consists of an NMOS transistor M3 and a PMOS resistor R1. By changing the PMOS resistance, various inductance value can be obtained.

Assuming the products $C_L \cdot C_{gs3}$ and $C_{gs3} \cdot C_{\mu 3}$ are negligible, then the impedance Z_L of the active inductor can be approximated by:

$$Z_L \approx \frac{1 + sR_1(C_{gs3} + C_{\mu 3})}{g_{m3} + s[g_{m3}R_1C_{\mu 3} + (C_{gs3} + C_L)]} \quad (7)$$

Where C_{gs3}, $C_{\mu 3}$ and C_L are the gate-source, gate-drain and load capacitances; g_{m3} is the transconductance of the transistor M3; and R1 is the PMOS resistance. If the condition

$$g_{m3} >> g_{m3}R_1C_{\mu 3} + (C_{gs3} + C_L) \quad (8)$$

is satisfied, then the inductive peaking is achieved.

The voltage gain of each cell is given by (9) [2].With poles and zero:

$$P_1 \approx \frac{g_{m3}}{g_{m3}R_1C_{\mu 3} + (C_{gs3} + C_L)} \quad (10)$$

$$P_2 \approx \frac{g_{m3}R_1C_{\mu 3} + (C_{gs3} + C_L)}{R_1[C_L(C_{gs3} + C_{\mu 3}) + C_{gs3}C_{\mu 3}]} \quad (11)$$

$$Z_p = \frac{1}{R_1(C_{gs3} + C_{\mu 3})} \quad (12)$$

From Equation (9), the dominant pole can be approximated by P_1 . Setting the zero equal to P_1, P_2 becomes the dominant pole and improves the bandwidth. The serious overshoot is prevented by selecting the Q-factor [3, 8]:

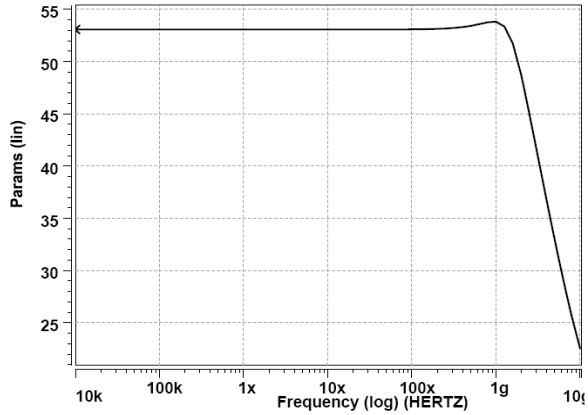
$$Q = \frac{\sqrt{g_{m3}R_1[C_L(C_{gs3} + C_{\mu 3}) + C_{gs3}C_{\mu 3}]}}{C_L + C_{gs3} + g_{m3}R_1C_{\mu 3}} = 0.7 \quad (13)$$

IV. SIMULATION RESULTS

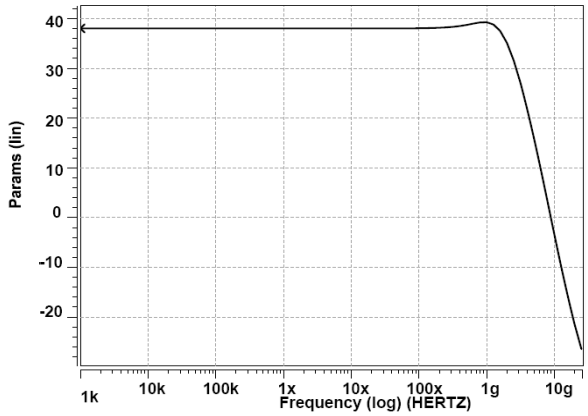
To verify the circuits performance, HSPICE software is used to simulate the proposed design using TSMC 0.18µm CMOS technology. A p-i-n photodiode with 250 fF capacitance was assumed as the input current source and was used as the input signal for the circuit simulations and supply voltage is 1.5V.

Fig. 5, shows the simulated frequency response of the TIA and LA. The figure reveals that the conversion gain and -3dB bandwidth of the TIA and the LA are 53dBΩ, 1.8GHz and 38dB, 2GHz respectively.

$$A = \frac{g_{m1}}{g_{m3}} \frac{1 + sR_1(C_{gs3} + C_{\mu 3})}{1 + s[g_{m3}R_1C_{\mu 3} + (C_{gs3} + C_L)]/g_{m3} + s^2R_1[C_L(C_{gs3} + C_{\mu 3}) + C_{gs3}C_{\mu 3}]/g_{m3}} \quad (9)$$



(a)



(b)

Fig. 6: Simulated frequency response: (a) TIA; (b) LA.

The time domain performance is verified by the transient simulation using the input current signal of about 100μA. Fig. 7 shows the transient response of LA. The figure reveals that the LA output voltage swing is 640mV.

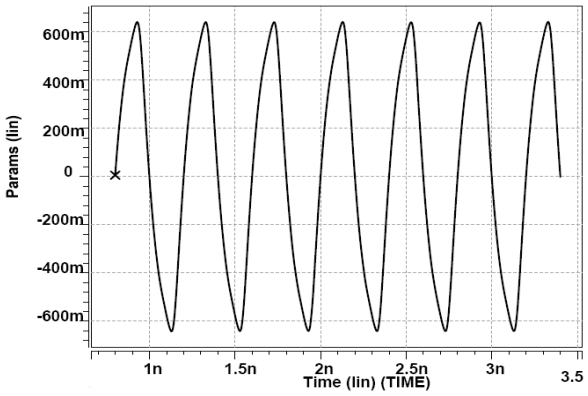


Fig. 7: Simulated transient response LA

Also power consumption is 794μW for TIA and 4mW for the LA, that is very lower with respect to other published designs.

Table I shows the comparison of the proposed design to results from several publishes optical receiver in CMOS technology.

TABLE I
comparison of the proposed design to other reported designs.

Design	**This Work**	[2]	[4]	[5]	[7]
Technology (CMOS)	**0.18 μm**	0.18 μm	0.25 μm	0.18 μm	0.18 μm
Data Rate (Gb/s)	**2.5**	2.5	2.5	2.5	8
TIA Gain (dBΩ)	**53**	66	48	61.9	50
LA Gain (dB)	**38**	29	-	-	46
TIA Bandwidth (GHz)	**1.8**	1.65	1.5	2	5.5
LA Bandwidth (GHz)	**2**	1.8	-	-	7.9
Power Supply (V)	**1.5**	3.3	2	1.5	1.8
TIA Power (mW)	**0.79**	10	74	2.6	112
LA Power (mW)	**4**	23		-	

V. CONCLUTION

High speed integrated optical communication systems will become increasingly ubiquitous given the continual increases in data volume and necessarily higher data transfer speeds.

In this paper design of optoelectronic amplifier consisting of the TIA and LA blocks using a TSMC 0.18μm CMOS technology, has been described and the HSPICE simulation results has been reported Using proposed design low power, large gain, high bandwidth, and high dynamic range can be achieved. Our proposed architecture is suitable as a low power building block for high performance optical interconnects and data communication systems.

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