An Active-Clamping ZVS Interleaved Buck/Boost Bidirectional Converter With One Auxiliary Switch

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***Abstract*—This article introduces a zero voltage switching (ZVS) interleaved buck/boost bidirectional converter using the active-clamp technique. In the proposed converter, by utilizing a simple auxiliary circuit comprised of an auxiliary switch, an auxiliary inductor, and a clamp capacitor, ZVS condition is secured for both the boost and buck operation modes, regardless of the converter operating duty cycle or load condition. Furthermore, the converter can operate with the conventional fixed-frequency pulsewidth modulation (PWM) control procedure. The boost and buck modes of the proposed converter are analyzed in both conditions of $D > 0.5$ and $D < 0.5$. To confirm the theoretical analysis, the experimental results of a 350 W–100 kHz prototype are presented.**

***Index Terms*—Active-clamping converter, interleaved bidirectional buck/boost converter (IBBC), pulsewidth modulation (PWM), zero voltage switching (ZVS).**

I. Introduction

THE N-PHASE interleaved bidirectional buck/boost converter (IBBC) is composed of N number of parallel bidirectional buck/boost converter (BBC) cells where the relative phase shift between the switching cells is 360°/N. This way, the current-ripple of the input source, which in many cases is the energy storage element, is either entirely or partially canceled, and the total volume of the converter inductors can reduce [1]. Due to the current sharing, the reliability improves [2], [3], thermal management becomes easier [4], and the total ohmic conduction losses (rI^2) reduces. In the bidirectional converters, the synchronous rectification is feasible, and so, the diode conduction losses could be negligible. Hence, in the N-phase IBBCs, the overall conduction losses are significantly reduced. Despite the desirable features of IBBC, the switching losses in an IBBC are almost the same with a single-phase BBC at a similar condition [5]. The switching losses restrict the possibility of increasing the converter switching frequency that is needed to increase the power density. Generally, the primary source of the switching losses in the bidirectional converters are the reverse recovery losses due to the slow body diode of the switches [5]. Also, since the capacitive turn-ON losses of switches are independent of the current value, when the number of phases in a hard-switching IBBC increases, the capacitive turn-ON losses would raise. Hence, utilizing soft-switching techniques featuring zero voltage switching (ZVS) is essential in IBBCs. Consequently, the excellent efficiency and high-frequency operation of the converter would achieve, simultaneously.

Compared to the single-phase or unidirectional converters, it is more challenging obtaining ZVS condition in an N-phase IBBC. An appropriate method to achieve ZVS in IBBCs is to design the main inductors in order to the converter can operate in the near-critical conduction mode (CRM) [6]–[12]. In this method, the ZVS condition is achieved without any auxiliary circuit. However, compared to when the converter operates in continuous conduction mode (CCM), the current ripple of the input source increases. Besides, in different conditions, to operate the converter at the optimum operating point, the approaches such as the variable frequency control methods [7]–[10], variable inductor [11], and variable coupling coefficient [12] should be applied which increases the cost and complexity.

In [13]–[15], the zero voltage transition (ZVT) method is used to obtain ZVS condition in IBBC while the converter can operate at CCM with the conventional fixed-frequency pulsewidth modulation (PWM) control procedure. However, in [13], [14], for each phase of IBBC, an independent auxiliary circuit including two auxiliary switches is utilized. Hence, for example in a two-phase IBBC, four auxiliary switches and many additional passive components are needed which increased the cost and complexity. Besides, in [15], although a single auxiliary inductor is used, still four auxiliary switches are needed to achieve ZVS condition in a two-phase IBBC. In [16]–[20], ZVT unidirectional interleaved converters with reduced auxiliary components are proposed. The main idea of these converters is that a single auxiliary ZVT cell is used to obtain ZVS condition of all phases through an additional diode for each phase. This method can develop to IBBCs. However, using this method for IBBCs still needs two auxiliary switches and two auxiliary diodes for each converter phase. Another approach to obtaining ZVS condition in IBBCs is developing the auxiliary circuits that proposed for the single-phase BBC [21]–[27]. For this purpose, each auxiliary circuit which proposed for a single phase BBC is utilized for each phase of IBBC. However, in this way, the

Manuscript received February 1, 2019; revised June 6, 2019 and August 22, 2019; accepted September 22, 2019. Date of publication October 8, 2019; date of current version April 30, 2020.

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Digital Object Identifier 10.1109/TIE.2019.2945284

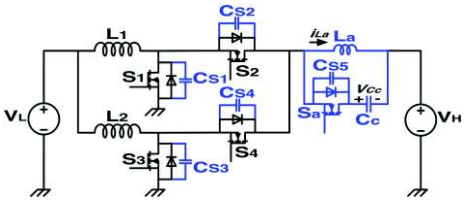

Fig. 1. Proposed ZVS active-clamping interleaved bidirectional buck/boost converter.

complexity and cost are increased. For example, to develop the auxiliary circuits of [21]–[27] to a two-phase IBBC, four auxiliary switches are required. Eventually, an important issue that should be noted is that in all the ZVS methods proposed in [13]–[26], albeit ZVS condition obtains for the main switches, the auxiliary switches turn-ON under zero current switching (ZCS). In fact, the capacitive turn-ON losses of the main switches transfer to the auxiliary switches, particularly if the voltage stress of the auxiliary switches is equal or more than the main switches. This issue increases the capacitive turn-ON losses in IBBC, mainly if the number of phases is increased.

In this article, a simple active-clamping circuit is proposed to provide the soft switching condition in a two-phase IBBC. The auxiliary circuit comprises an auxiliary switch, an auxiliary inductor, and an auxiliary capacitor. In the proposed converter, the ZVS condition is achieved for all the main switches and auxiliary switch at both the turn-ON and turn-OFF instants, regardless of the operating duty cycle value, power flow direction or load condition. Furthermore, in the proposed method, there is no need for the complex variable-frequency control methods, and IBBC can operate with the conventional fixed-frequency PWM control procedure. In Section II, the converter structure is described, and the operation of the converter is presented for both boost and buck modes at the conditions of $D > 0.5$ and $D < 0.5$. In Section III, design considerations are given. In Section IV, the experimental results of a 350 W-100 kHz prototype for both the boost and buck modes in full load, 30% of full load and 10% of full load are presented. Finally, Section V concludes this article.

II. Circuit Description and Operation

Fig. 1 depicts the proposed active-clamping IBBC. As seen, the auxiliary circuit is comprised of an auxiliary switch S_a, an auxiliary inductor L_a, and a clamp capacitor C_C. Besides, the capacitors C_{S1}, C_{S2}, C_{S3}, C_{S4}, and C_{S5} are the snubber capacitors of the switches. Based on the power flow direction, the proposed converter has two operation modes of boost and buck modes. In each operation mode, depending on whether the operating duty cycle is more than 0.5 or not, the converter operates in two conditions of $D > 0.5$ and $D < 0.5$. This section discusses the converter operation in both conditions. To simplify the theoretical analysis, the following assumptions are made:

- The converter operates at steady-state condition, and the elements are ideal.
- The inductors L_1 and L_2 and the capacitor C_C are fairly large so that, I_{L1}, I_{L2}, and V_{Cc} are constant in a switching cycle.

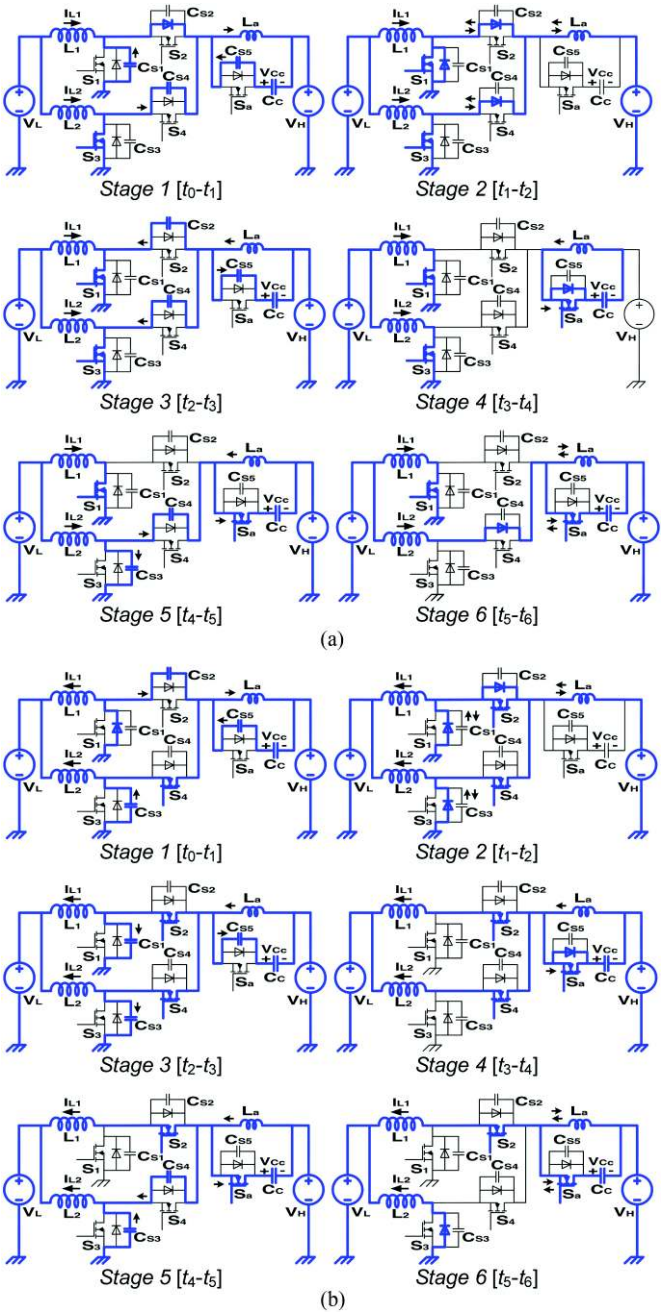

Fig. 2. Equivalent circuits of half-cycle operating stages for $D > 0.5$. (a) Boost mode. (b) Buck mode.

At both the conditions of $D > 0.5$ and $D < 0.5$, the converter involves twelve operating stages in both the boost and buck modes. Regardless of the converter operating condition, the converter operation consists of two symmetrical half-cycles during each switching period. Therefore, in each condition, solely half of the switching cycle is explained.

A. Condition I: $D > 0.5$

Fig. 2 illustrates the equivalent circuits of the half-cycle operating stages for $D > 0.5$ in the boost and buck modes. Besides, Fig. 3 depicts the fundamental waveforms of the converter in

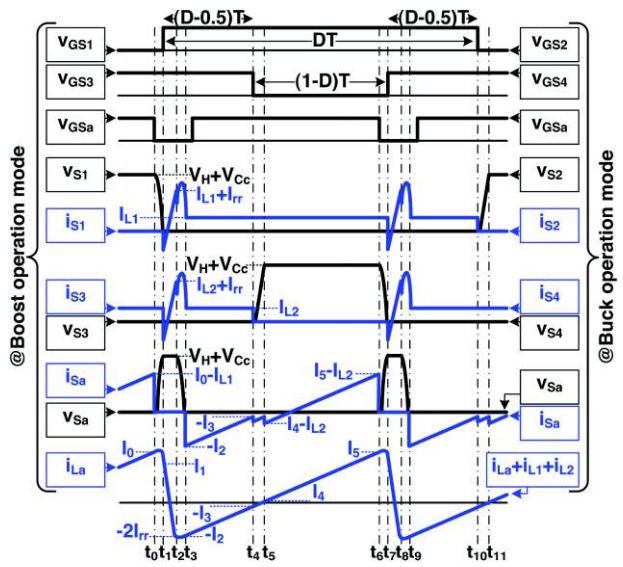

Fig. 3. Converter fundamental waveforms for $D > 0.5$.

this condition. Since the operation of the auxiliary circuit and the theoretical equations in both boost and buck modes are almost similar, only the boost mode is discussed. In boost mode, the main switches S_1 and S_3 are controlled, and power flows from V_L to V_H. Besides, the main switches S_2 and S_4 are OFF, and their body diodes serve as the converter rectifying diodes.

Before the first stage, it is assumed that S_1 is OFF, and so, I_{L1} conducts through the S_2 body diode. Besides, S_3 and S_a are ON, and the L_a current value is defined as I_0. Note that, L_a current direction determines according to the current arrow shown in Fig. 1.

Stage 1. [t_0–t_1]: At t_0, the auxiliary switch S_a turns OFF under ZVS condition, due to the snubber capacitor C_{S5}, C_{S1}, and C_{S4}. At the same time, a resonance starts between L_a, C_{S1}, C_{S4}, and C_{S5}. During this resonance, C_{S1} and C_{S4} discharges from $V_H + V_{Cc}$ to zero, and C_{S5} charges to $V_H + V_{Cc}$. At t_1, L_a current value is defined as I_1. In this stage, the voltage equation of S_1 would be

$$v_{S1} = V_H + V_{Cc}\cos(\omega_0(t-t_0)) + Z_0(I_{L1}-I_0)\sin(\omega_0(t-t_0)) \quad (1)$$

where

$$\omega_0 = 1/\sqrt{L_a(C_{S1}+C_{S4}+C_{S5})},$$
$$Z_0 = \sqrt{L_a/(C_{S1}+C_{S4}+C_{S5})}.$$

Stage 2. [t_1–t_2]: At t_1, the body diodes of S_1 and S_4 turn-ON under ZVS condition. Hence, the main switch S_1 turn ON under ZVS condition. During this stage, the voltage of L_a is clamped by -V_H and so, L_a current equation is as follows:

$$i_{La} = I_1 - \frac{V_H}{L_a}(t-t_0). \quad (2)$$

According to (2), L_a current declines to zero, while the inductor L_a restricts the current reduction rate of the S_2 and S_4 body diodes at turn-OFF. After that, the reverse recovery of S_2 and S_4 body diodes begin. At t_2, L_a current is equal to the sum of S_2 and S_4 body diodes reverse recovery currents ($-2I_{rr}$).

Stage 3. [t_2–t_3]: In this stage, C_{S2} and C_{S4} charge to $V_H + V_{Cc}$, due to a resonance between L_a, C_{S2}, C_{S4} and C_{S5}. In this stage, the current equation of S_1 would be

$$i_{S1} = I_{L1} + \frac{2I_{rr}C_{S2}}{C_{S2}+C_{S4}+C_{S5}}\cos(\omega_1(t-t_2)) + C_{S2}\omega_1 V_H \sin(\omega_1(t-t_2)) \quad (3)$$

where $\omega_1 = 1/\sqrt{L_a(C_{S2}+C_{S4}+C_{S5})}$. At t_3, L_a current value is defined as $-I_2$.

Stage 4. [t_3–t_4]: At t_3, the S_a body diode turns ON under ZVS condition, and L_a current is flowing through it. In this condition, the auxiliary switch S_a turns ON under ZVS condition. Meanwhile, the voltage of L_a is clamped by V_{Cc}. Hence, L_a current linearly diminishes as follows:

$$i_{La} = -I_2 + \frac{V_{Cc}}{L_a}(t-t_3). \quad (4)$$

At t_4, L_a current value is defined as $-I_3$.

Stage 5. [t_4–t_5]: At t_4, the main switch S_3 turns OFF under ZVS condition due to the snubber capacitors C_{S3} and C_{S4}. After that, the snubber capacitors C_{S3} and C_{S4} charge to $V_H + V_{Cc}$. Hence, the voltage equation of S_3 would be

$$v_{S3} = \frac{I_{L2}}{C_{S3}+C_{S4}}(t-t_4). \quad (5)$$

At t_5, L_a current value is defined as I_4.

Stage 6. [t_5–t_6]: In this stage, the S_4 body diode conducts I_{L2}. Hence, the difference current of i_{La} and I_{L2} ($i_{La} - I_{L2}$) conducts through S_a. Similar to stage 4, the voltage of L_a is clamped by V_{Cc}, and L_a current linearly increases. Hence, S_a current decreases to zero and then, increases in the opposite direction. The S_a current equation is as follows:

$$i_{Sa} = I_4 - I_{L2} + \frac{V_{Cc}}{L_a}(t-t_5). \quad (6)$$

At the end of this stage, L_a current is defined as I_5. At t_6, the auxiliary switch S_a turns OFF, and the next half of the switching cycle begins. The next sequence is similar to the operation of the previous half-period, such as from stages 1 to 6.

B. Condition II: $D < 0.5$

Fig. 4 depicts the equivalent circuits of the half-cycle operating stages for $D < 0.5$ in the boost and buck modes. Besides, Fig. 5 illustrates the fundamental waveforms of the converter in this condition. Since the operation of the auxiliary circuit and the theoretical equations in both boost and buck modes are almost similar, solely the boost mode is discussed. Before the first stage, it is assumed that S_1 and S_3 are OFF and so, I_{L1} and I_{L2} conduct through the body diodes of S_2 and S_4, respectively. Besides, S_a is ON, and L_a current value is defined as I_0.

Stage 1. [t_0–t_1]: At t_0, the auxiliary switch S_a turns OFF under ZVS condition due to the snubber capacitors C_{S5}, C_{S1}, and C_{S3}. After that, a resonance starts between L_a, C_{S1}, C_{S3},

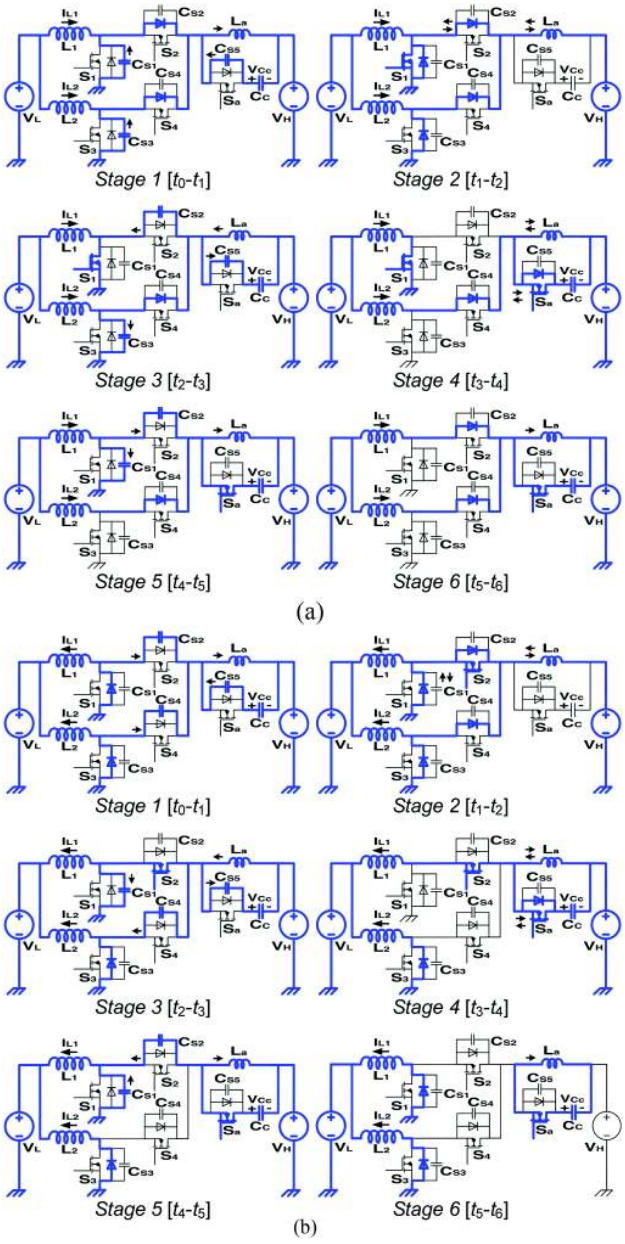

Fig. 4. Equivalent circuits of half-cycle operating stages for $D < 0.5$. (a) Boost mode. (b) Buck mode.

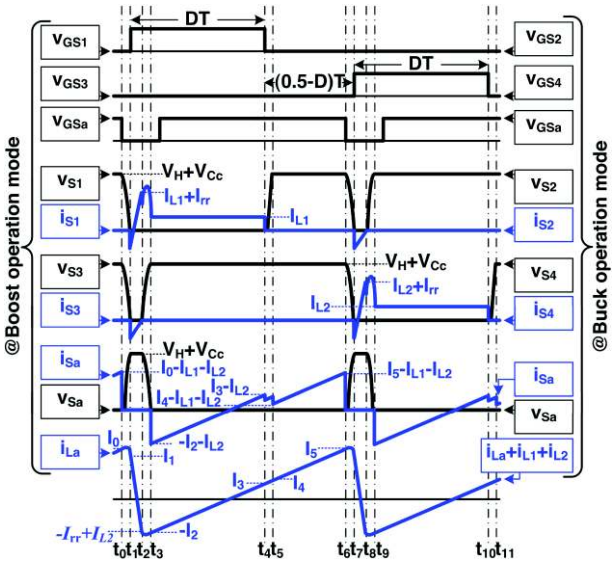

Fig. 5. Converter fundamental waveforms for $D < 0.5$.

and C_{S5}. During this resonance, the snubber capacitor C_{S5} charges to $V_H + V_{Cc}$, and the snubber capacitors C_{S1} and C_{S3} discharge from $V_H + V_{Cc}$ to zero. In this condition, the voltage equation of S_1 would be

$$v_{S1} = V_H + V_{Cc}\cos(\omega_2(t-t_0)) + Z_1(I_{L1}+I_{L2}-I_0)\sin(\omega_2(t-t_0)) \quad (7)$$

where $\omega_2 = 1/\sqrt{L_a(C_{S1}+C_{S3}+C_{S5})}$, $Z_1 = \sqrt{L_a/(C_{S1}+C_{S3}+C_{S5})}$.

At t_0, L_a current value is defined as I_1.

Stage 2 [t_1–t_2]: In this stage, the body diodes of S_1 and S_3 turn ON and so, the main switch S_1 can turn ON under ZVS condition. During this stage, the voltage of the auxiliary inductor L_a is clamped by -V_H and L_a current decreases to zero. Then the reverse recovery of S_2 body diode begins. The L_a current equation is

$$i_{La} = I_1 - \frac{V_H}{L_a}(t-t_0). \quad (8)$$

According to (8), the inductor L_a restricts the current reduction rate of the S_2 body diode at turn-OFF. At the end of this stage, L_a current value is $-I_{rr} + I_{L2}$.

Stage 3. [t_2–t_3]: In this stage, a resonance starts between L_a, C_{S2}, C_{S3}, and C_{S5}. During this resonance, C_{S5} discharges to zero, and, C_{S2} and C_{S3} charge to $V_H + V_{Cc}$. In this stage, the current equation of S_1 is

$$i_{S1} = I_{L1} + \frac{I_{rr}C_{S2}}{C_{S2}+C_{S3}+C_{S5}}\cos(\omega_3(t-t_2)) + C_{S2}\omega_4 V_H \sin(\omega_3(t-t_2)) \quad (9)$$

where $\omega_3 = 1/\sqrt{L_a(C_{S2}+C_{S3}+C_{S5})}$. At t_3, L_a current value is defined as $-I_2$.

Stage 4. [t_3–t_4]: At t_3, the S_a body diode turns ON under ZVS condition and so, the auxiliary switch S_a turns ON under ZVS condition. During this stage, the voltage of L_a is clamped by V_{Cc}. Hence, according to (10), L_a current decreases linearly to zero and then increases in the opposite direction.

$$i_{La} = -I_2 + \frac{V_{Cc}}{L_a}(t-t_3). \quad (10)$$

Besides, the difference current of i_{La} and I_{L2} $(i_{La} - I_{L2})$ is flowing through S_a. At t_4, L_a current value is defined as I_3.

Stage 5. [t_4–t_5]: At t_4, the main switch S_1 turns OFF under ZVS condition due to snubber capacitors C_{S1} and C_{S2}. After that, C_{S1} and C_{S2} charge to $V_H + V_{Cc}$. Hence, the voltage equation of S_1 would be

$$v_{S1} = \frac{I_{L2}}{C_{S1}+C_{S2}}(t-t_4). \quad (11)$$

At t_5, L_a current value is defined as I_4.

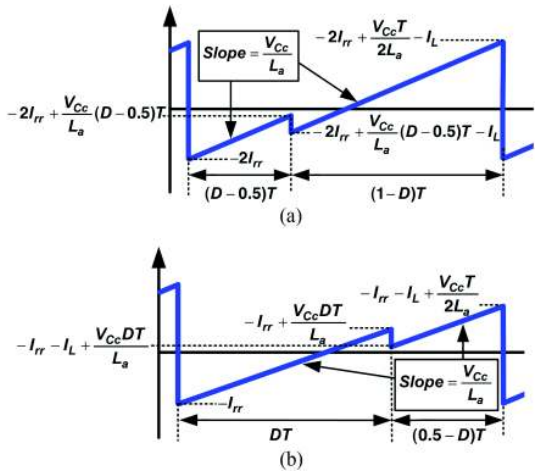

Fig. 6. Auxiliary switch current waveforms (i_{Sa}) of the simplified operation. (a) $D > 0.5$. (b) $D < 0.5$.

Stage 6. [t_5–t_6]: In this stage, the S_2 body diode turns ON under ZVS condition, and so, I_{L1} is flowing through it. Hence, the difference current of i_{La} and $I_{L1} + I_{L2}$ ($i_{La} - I_{L1} - I_{L2}$) is flowing through S_a. Similar to stage 4, the voltage of L_a is clamped by V_{Cc}, and so, L_a current increases linearly. At t_6, L_a current value is defined as I_5. At t_6, the auxiliary switch S_a turns OFF, and the next half of the switching cycle begins. The next sequence is similar to the operation of the previous half-period, such as from stages 1 to 6.

III. Design Considerations

This section presents the design considerations of the proposed converter. To simplify the theoretical analysis, it is assumed that the snubber capacitors are equal ($C_{S1} = C_{S2} = C_{S3} = C_{S4} = C_{S5} = C_S$). Besides, the currents of the inductors L_1 and L_2 are supposed to be equal ($I_{L1} = I_{L2} = I_L$).

A. V_{Cc} and I_0 Calculation

As discussed, V_{Cc} is the voltage value of the capacitor C_C, and I_0 is the current value of L_a at the beginning of stage 1. These values have an important role in ZVS condition and additional voltage stress of the main switches. To obtain the values of I_0 and V_{Cc}, some simplifications are necessary; otherwise, the relations would become cumbersome. Compared to the switching period, the duration time of the commutation and resonance stages (stages 1, 2, 3, and 5) is short and can be omitted. This way, the converter operation is simplified by two stages, 4 and 6. Fig. 6 illustrates the auxiliary switch current waveforms of the simplified operation for both conditions of $D > 0.5$ and $D < 0.5$. Consequently, I_0 and V_{Cc} are obtained from this analysis. From Fig. 6, when $D > 0.5$, I_0 is derived as follows:

$$I_0 = -2I_{rr} + (V_{Cc}T)/2L_a \tag{12}$$

Besides, when $D < 0.5$, I_0 is

$$I_0 = -I_{rr} + (V_{Cc}T)/2L_a \tag{13}$$

At the steady-state condition, the average current of the clamp capacitor is zero. Since $i_{Cc} = -i_{Sa}$, and from Fig. 6(a), V_{Cc} when $D > 0.5$ is obtained as follows:

$$V_{Cc} = \frac{8L_a}{T}[I_{rr} + I_L(1-D)]. \tag{14}$$

Similarly, from Fig. 6(b), V_{Cc} when $D < 0.5$ is

$$V_{Cc} = \frac{4L_a}{T}[I_{rr} + I_L(1-2D)]. \tag{15}$$

B. ZVS Condition

To achieve ZVS condition for the main switches in turn-ON instant, at the end of stage 1, the voltage of the main switches must reach zero. Hence, before stage 1, the stored energy in L_a should be sufficient to discharge or charge the snubber capacitors. Thus, the following condition should satisfy:

$$\frac{1}{2}(L_a)(I_0)^2 > 3\left(\frac{1}{2}C_S(V_H + V_{Cc})^2\right) \tag{16}$$

where V_{Cc} is the voltage value of C_C, and I_0 is the current value of L_a at the beginning of stage 1. From (16), the ZVS condition formulates as follows:

$$I_0 > (V_H + V_{Cc})/Z_2 \tag{17}$$

where $Z_2 = \sqrt{L_a/3C_S}$. From (12), (14), and (17), and assuming $V_H \gg V_{Cc}$, the following ZVS condition for the condition of $D > 0.5$ is achieved:

$$2I_{rr} + 4I_L(1-D) > V_H/Z_2. \tag{18}$$

Similarly, from (13), (15), and (17), ZVS condition for the condition of $D < 0.5$ is obtained as

$$I_{rr} + 2I_L(1-2D) > V_H/Z_2. \tag{19}$$

Consequently, to achieve the ZVS condition for the main switches at turn-ON, the requirements of (18) and (19) must satisfy. Note, the above conditions are valid in both boost and buck modes of operation. As seen in ZVS conditions of (18) and (19), the reverse recovery current of the switches body diodes (I_{rr}) is effective in ZVS condition. From [28], I_{rr} is

$$I_{rr} = \sqrt{Q_{rr}\frac{di}{dt}} \tag{20}$$

where, Q_{rr} and *di/dt* are the reverse recovery charge and the current reduction rate of the diode at turn-OFF, respectively. Q_{rr} is the inherent feature of the diode, and its maximum value at the maximum current rating of the diode obtains from the manufacturer data sheet. The actual value of Q_{rr} at the converter operating point can be estimated as follows [29]:

$$Q_{rr} = Q_{rr\_spec}\sqrt{I_L/I_{F\_spec}} \tag{21}$$

where Q_{rr_spec} is the maximum value of Q_{rr}, and I_{F_spec} is the maximum current rating of the diode, presented in diode datasheet. Besides, I_L is the average current of each main inductor. Furthermore, the auxiliary circuit determines *di/dt*. Hence, from stage 1, when $D > 0.5$, we have

$$di/dt = V_H/2L_a. \tag{22}$$

And when $D < 0.5$, *di/dt* is

$$di/dt = V_H / L_a. \tag{23}$$

According to (18) and (19), the worst-case condition of ZVS operation is when $D < 0.5$ and the converter operates in light loads. In this condition, and from (19), if $I_{rr} > V_H / Z_2$, the ZVS operation is obtained for the other operating points. Hence, from this requirement, and (20), (21), and (23), the following ZVS condition is obtained

$$C_S < C_{S\_\max} = \frac{Q_{rr\_spec}}{3V_H} \sqrt{\frac{I_L}{I_{F\_spec}}}. \tag{24}$$

Note, I_L should be calculated in the condition that the converter operates in light loads. Consequently, if the snubber capacitor of each switch (C_S) is selected according to (24), the ZVS operation of the converter in the whole operating points is secured. It should be noted that, according to (3) and (9), the snubber capacitors values are effective in the current peak value of the main switches, and also auxiliary switch. Hence, to obtain ZVS condition on a wide range of loads with the minimum conduction losses, it is desirable to select the minimum value of the snubber capacitors. The minimum value of the snubber capacitors is calculated like any snubber capacitor [30]. Note that, according to (5) and (11), and from stage 1, the equivalent values of the snubber capacitors for each main switch and auxiliary switch are equal to $2C_S$ and $3C_S$, respectively. Hence, it is feasible to select a lower value for the snubber capacitors.

C. Limiting the Additional Voltage Stress

As seen in the analysis of the proposed converter, the additional voltage stress of the main switches is equal to the voltage of capacitor C_C (V_{Cc}). From (14) and (15), in the condition of $D > 0.5$ and full load, the value of V_{Cc} is maximized. Hence, from (14), (20), and (22), to limit the V_{Cc} to below 30% of V_H, the following condition should be satisfied:

$$L_a < L_{a\_\max} = \frac{0.01 V_H}{f^2 Q_{rr}} \left(\frac{1}{1 + \sqrt{1 + \frac{0.15 P_o}{f Q_{rr} V_H}}} \right)^2 \tag{25}$$

where f and P_o are the converter switching frequency and maximum output power, respectively. Note, Q_{rr} should be calculated from (21), when $D > 0.5$ and converter operates in full load. Consequently, if the value of inductor L_a is selected as (25), the additional voltage stress of the switches (V_{Cc}) always limits to below $0.3\ V_H$. Based on (20), (22), and (23), to reduce the value of $I_{\rm rr}$ and so, the additional conduction losses of the proposed converter, it is desirable to select the maximum value of L_a $(L_{a\_\max})$.

D. Control of the Proposed Converter

Generally, in a basic IBBC, to maintain the current balancing between the phases, and also to control the total current value of phases, the current mode control methods should be applied. Fig. 7(a) illustrates the control block diagram of the proposed converter, which consists of a conventional PWM current mode

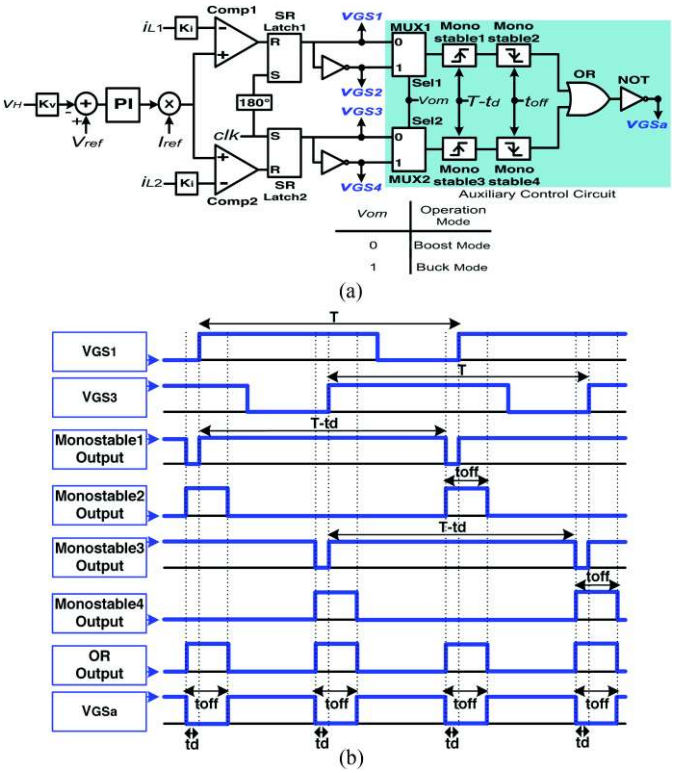

Fig. 7. (a) Control block diagram of the control circuit. (b) Key waveforms of the auxiliary control circuit in boost mode.

controller (featuring peak current mode control) and the auxiliary control circuit. The role of the auxiliary control circuit is generating the proper pulse from the main control unit for the auxiliary switch. A typical way to generate a synchronized pulse with a controlled pulsewidth (t_{pw}) and controlled delay time (t_d) is the use of two series monostables. To illustrate the operation of the auxiliary control circuit, the key waveforms of the auxiliary circuit control in the boost mode are shown in Fig. 7(b). As seen, the pulsewidth of the monostables 1 and 3 adjusts the delay time between the auxiliary switch turn-OFF and the main switches turn-ON (t_d). Besides, the pulsewidth of monostables 2 and 4 adjusts the OFF-state time of the auxiliary switch $(t_{\rm off})$.

IV. Experimental Results

To verify the proper operation of the proposed IBBC, a laboratory prototype is implemented. Table I shows the values of parameters and the components of the prototype converter. The high-voltage level of the implemented prototype is the down-scaled voltage level (with a ratio of about 0.5) of a dc-bus voltage with the conventional value of about 380 V.

For all switches, the MOSFET IRFP350 is used which its body diode specs are $Q_{rr_spec} = 8.1\ \mu$C and $I_{F\_spec} = 15$ A. To secure ZVS condition in a wide range of full load to 10% of full load, from (24) and by putting I_L equal to 0.25 A (I_L in 10% of full load), $C_{S\_\max}$ is obtained 1.7 nF. For the snubber capacitors, the output capacitors (C_{oss}) of the switches are used

TABLE I
PARAMETERS AND COMPONENT VALUES OF THE IMPLEMENTED PROTOTYPE CONVERTER

Symbol	Parameter	Value
P_o	Output power	350 W
V_H	High-voltage side	200 V
V_L	Low-voltage side	70 V
f	Switching frequency	100 kHz
L_1, L_2	Main inductors	2 mH
L_a	Auxiliary inductor	10 μH
C_C	Clamp capacitor	2.2 μF
$C_{S1}, C_{S2}, C_{S3}, C_{S4}, C_{S5}$	Snubber capacitors	660 pF*

*Output capacitor (C_{oss}) of MOSFET IRFP350

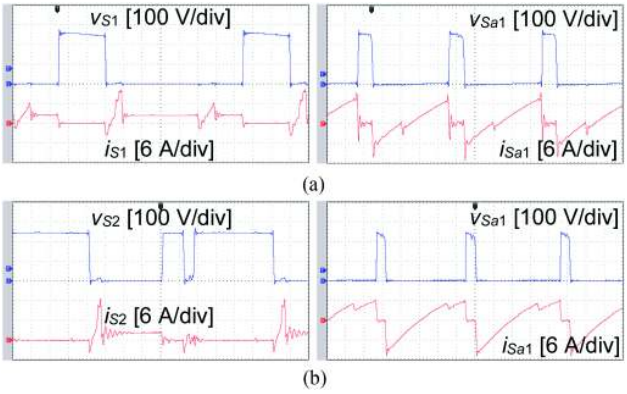

Fig. 8. Experimental results at full load (350 W). (a) Boost operation. (b) Buck operation (time scale is 1 μs/div).

$(C_S = C_{oss} = 660\text{pF})$. Besides, from (25) and (21), $L_{a\_\max}$ is obtained 11 μH. L_a is selected equal to 10 μH. The control circuit is implemented using the UCC2822 interleaved dual PWM controller.

A. Experimental Waveforms Description

The measured waveforms of the main switches of the upper phase (S_1 in boost mode and S_2 in buck mode) and the auxiliary switch (S_a) at full load (350 W), 30% of full load (100 W), and 10% of full load (35 W) are illustrated in Figs. 8, 9, and 10, respectively. As seen, ZVS condition for all the main and auxiliary switches of the converter is obtained for a wide range of loads, and with a fixed switching frequency. These features achieve for both the condition of $D = 0.65$ (boost mode) and $D = 0.35$ (buck mode).

To verify the proper operation of the proposed converter in a wide range of duty cycles, the measured waveforms of the main switches in operating point of $V_L = 30$ V, $V_H = 200$ V, and $P_o = 100$ W are shown in Fig. 11. In this operating point, the theoretical duty cycles of boost and buck modes are 0.85 and 0.15, respectively. As seen, the ZVS condition is secured in a very large or small value of duty cycles. The above features are achieved by using only one auxiliary switch. Table II presents a comparison between the proposed IBBC and another soft switching IBBCs. To show the transient performance of the proposed converter, the high-voltage side voltage (v_H) and the

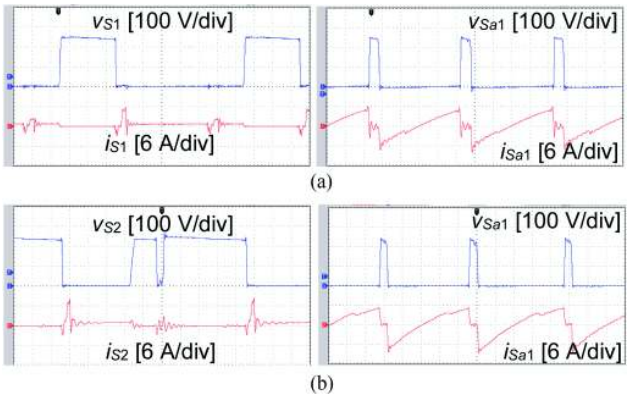

Fig. 9. Experimental results at 30% of full load (100 W). (a) Boost operation. (b) Buck operation (time scale is 1 μs/div).

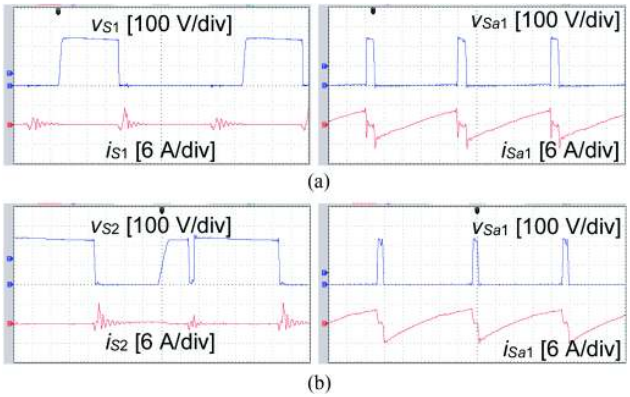

Fig. 10. Experimental results at 10% of full load (35 W). (a) Boost operation. (b) Buck operation (time scale is 1 μs/div).

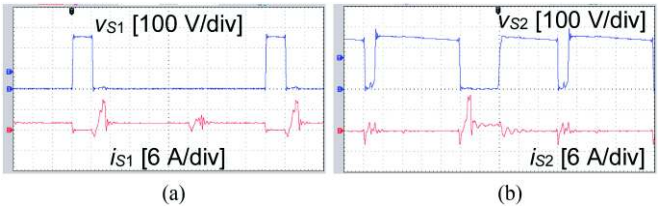

Fig. 11. Experimental results in operating point of $V_L = 30$ V, $V_H = 200$ V, and $P_o = 100$ W. (a) Boost operation ($D = 0.85$). (b) Buck operation ($D = 0.15$) (time scale is 1 μs/div).

total input currents $(i_{L1} + i_{L2})$ are measured in boost mode (worst case operation mode) at the alternating condition of light load (35 W) to heavy load (350 W) and vice versa. The measured waveforms are illustrated in Fig. 12.

B. Power Losses Analysis

To analyze further the effectiveness of the proposed converter, a losses breakdown analysis is undertaken. Due to the fully ZVS operation of the proposed converter, the switching losses are almost eliminated, and the conduction and core losses are evaluated. Table III presents the measured power losses in different conditions.

TABLE II
COMPARISON BETWEEN THE PROPOSED IBBC AND ANOTHER SOFT SWITCHING IBBCS

	ZVT IBBC in [13]	ZVT IBBC in [14]	ZVT IBBC in [15]	**Proposed IBBC**
Number of auxiliary switch(es)	4	4	4	**1**
Number of auxiliary passive element(s)	2	18	1	**2**
Main switches turn-ON condition	ZVS	ZCS	ZVS	**ZVS**
Main switches turn-OFF condition	ZVS	ZVS	ZVS	**ZVS**
Auxiliary switch(es) turn-ON condition	ZCS	ZCS	ZCS	**ZVS**
Auxiliary switch(es) turn-OFF condition	ZCS	ZCS	ZCS	**ZVS**

Note: The comparison is between the two-phase IBBCs counterpart.

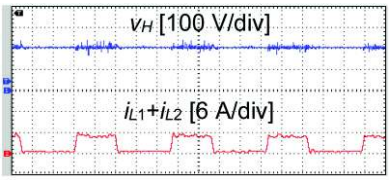

Fig. 12. Transient performance of the proposed converter in boost mode through the condition of light load (35 W) to heavy load (350 W) (time scale is 25 ms/div).

TABLE III
POWER LOSS ANALYSIS OF THE PROPOSED CONVERTER

	S_1 & S_3 Conduction Loss	S_2 & S_4 Conduction Loss	S_a Conduction Loss	L_1 & L_2 Copper Loss	L_a Copper Loss	L_a Core Loss	Other Losses	Total Losses	**Efficiency**
Boost Mode P_o=350W	3.46 W	1.43 W	4.42 W	3.75 W	1.27 W	1.13 W	0.3 W	15.76 W	**95.5 %**
Boost Mode P_o=100W	0.55 W	0.48 W	2.48 W	0.31 W	0.71 W	0.27 W	0.3 W	5.1 W	**94.9 %**
Boost Mode P_o=35W	0.14 W	0.10 W	1.73 W	0.04 W	0.50 W	0.21 W	0.3 W	3.02 W	**91.4 %**
Buck Mode P_o=350W	2.16 W	2.62 W	5.60 W	3.75 W	1.61 W	0.67 W	0.3 W	16.71 W	**95.2 %**
Buck Mode P_o=100W	0.67 W	0.83 W	3.38 W	0.31 W	1.00 W	0.27 W	0.3 W	6.76 W	**93.2 %**
Buck Mode P_o=35 W	0.21 W	0.31 W	2.10 W	0.04 W	0.60 W	0.15 W	0.3 W	3.71 W	**89.4 %**

The switches conduction losses and the inductor copper losses are obtained from $R_{\mathrm{DS(on)}}\, I^2_{\mathrm{RMS\_Switch}}$ and $R_{\mathrm{DC}} I^2_{\mathrm{RMS\_Coil}}$, respectively. $R_{\mathrm{DS(on)}}$ is the ON-state resistance of the switches ($R_{\mathrm{DS(on)}} = 450$ mΩ in junction temperature (T_j) of 75°), and R_{DC} is the total copper resistance of the inductor coil ($R_{\mathrm{DC\_La}} = 60$ mΩ, $R_{\mathrm{DC\_}L1} = 300$ mΩ and $R_{\mathrm{DC\_}L1} = 300$ mΩ). Besides, $I_{\mathrm{RMS\_Switch}}$ and $I_{\mathrm{RMS\_Coil}}$ are the root-mean-square (rms) value of the switch and inductor current, respectively. The rms values of currents in different conditions are measured from the experimental results waveforms.

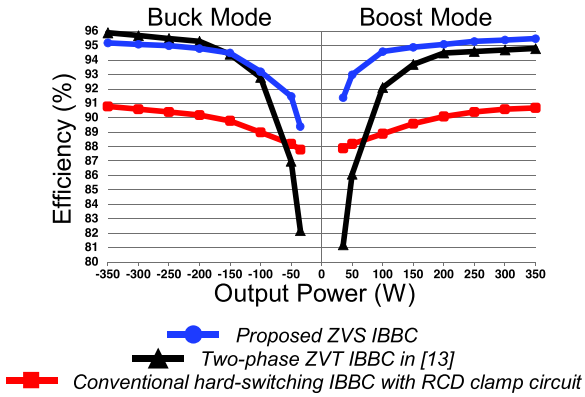

Fig. 13. Efficiency curves of the proposed IBBC, two-phase ZVT IBBC in [13], and the conventional IBBC with RCD clamp circuit under the condition of $V_L = 70$ V, $V_H = 200$ V, and f = 100 kHz.

The core losses are obtained from the Steinmetz equation, which is the conventional equation for estimating the core losses [5], [31], [32]. The Steinmetz equation is as follows:

$$P_C = a f^x (B_{pk})^y \tag{26}$$

where P_C is the core loss density in mW/cm^3, f is the switching frequency in Hertz, and B_{pk} is the peak flux density in Tesla ($B_{pk} = \Delta B/2$). Besides, a, x, and y are the Steinmetz coefficients provided by the manufacturer. The value of B_{pk} in the linear region is obtained as follows [31]:

$$B_{pk} = \frac{\Delta B}{2} = \frac{L \Delta i}{2 n A_e} \tag{27}$$

where, L is the inductor value, Δi is the inductor current swing, n is the number of winding turns, and A_e is the core effective cross-sectional area. From, (26) and (27), and by multiplying P_C in V_e (effective core volume), the core loss is estimated. For L_a, the ferrite core EI25/19 ($A_e = 42$ mm^2, $V_e = 2.04$ cm^3) with an air gap and 14 turns of winding is used, and for the main inductors L_1 and L_2, the ferrite core EE42/42/15 ($A_e = 182$ mm^2, $V_e = 17.6$ cm^3) with an air gap and 91 turns of winding is applied. Based on the selected core, the Steinmetz coefficients are selected as $a = 3.75 * 10^{-3}$, $x = 1.42$, and $y = 2.88$. Note, in the main inductors L_1 and L_2, since Δi is very small, the core loss of each inductor is derived 3.7 mW. Hence, the values of core loss in L_1 and L_2 are omitted in Table III. Finally, the efficiency curves of the proposed ZVS IBBC in comparison with two-phase ZVT IBBC in [13], and the conventional hard-switching IBBC using the resistor-capacitor-diode (RCD) clamp circuit are illustrated in Fig. 13. Generally, in ZVT IBBCs, by the cost of using four auxiliary switches, the ZVS condition of the main switches is obtained with the minimum circulating current and no additional voltage stress on the main switches. However, in these converters, as shown in Table II, the auxiliary switches turn-ON under ZCS. As a result, there is a constant capacitive turn-ON loss in the converter which reduces the efficiency, especially at light loads.

V. Conclusion

A ZVS interleaved bidirectional buck/boost converter was introduced. By using a simple auxiliary circuit composed of an auxiliary switch, an auxiliary inductor, and a clamp capacitor, ZVS condition was secured for both the boost and buck modes of the converter. The proposed converter operated with conventional fixed-frequency PWM control methods. The proposed converter was fully analyzed in both the buck and boost modes at the conditions of $D > 0.5$ and $D < 0.5$. Besides, the design considerations of the proposed converter, including the simplified operation analysis of the converter, was presented. The experimental results of a 350 W–100 kHz prototype were presented for both the boost and buck operations at full load, 30% of full load (100 W) and 10% of full load (35 W). The experimental results confirmed the proper operation of the proposed converter.

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