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ORIGINAL RESEARCH

An energy-efficient dynamic comparator in Carbon Nanotube Field Effect Transistor technology for successive approximation register ADC applications

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Abstract

In this paper, a latch-based energy-efficient dynamic comparator is presented in Carbon Nanotube Field Effect Transistor (CNTFET) technology. The proposed comparator consists of two main stages: pre-amplifier and latch. The latch stage is designed for the main purpose of low-power consumption and high-speed performances. The proposed speed-up technique for the latch structure controls the threshold voltage (V_{th}) of the cross-coupled inverters. So, the delay of the latch stage decreases and consequently, the overall delay of the comparator circuit is also reduced up to 19.4% while the maximum speed performance of the proposed comparator increases by 54% compared to the conventional double-tail dynamic comparator. Additionally, the use of the proposed distinctive structure for the tail transistors in the latch stage, leads to more than 11% reduction in the energy per conversion of the proposed circuit compared to the conventional double-tail dynamic comparator. To verify the circuit performances, the comparator circuit is simulated in HSPICE using 32 nm CNTFET Stanford model technology parameters. The simulation results show that the proposed comparator with the proposed speed-up approach can operate up to 14.2 GHz with a sensitivity of 30 μV at the supply voltage of 1 V, while consumes only 42.38 μW of power. Therefore, the proposed comparator can be used in high-resolution (up to 12 bit) and high-speed low-power analogue-to-digital converter applications. Moreover, the effects of the non-ideal fabrication process (including the pitch and the threshold voltage variations), supply voltage and temperature variations are investigated in this work. Monte-Carlo analysis shows that the standard deviation of the offset voltage is approximately 1.24 mV. Finally, the kickback noise of the proposed comparator is obtained as 80 μV, which shows the proper performance of the proposed comparator circuit in comparison with other reported designs.

KEYWORDS

analogue-to-digital converter (ADC), CNTFET, dynamic comparator, high-speed, low-power

1 | INTRODUCTION

Comparators are considered as the important building blocks in data converters, such as successive approximation register (SAR) and pipe-line analogue-to-digital converters (ADCs). Among different types of comparators, dynamic comparators which are working based on the positive feedback structure are very popular and have many applications in the recent ADC circuits. Moreover, these comparators benefit from the lower power consumption than other types of comparators and are preferred

in many new types of data converters, such as novel flash, pipe-line and SAR ADCs [1]. Based on their application, a pre-amplifier stage is sometimes added to the comparator structure to extend the voltage difference between the two input signals to achieve a higher resolution [1]. Besides power consumption, other parameters such as speed, sensitivity (comparator accuracy), input-referred voltage error and kickback noise, are considered as the major performance measures for the performance comparison of different comparator topologies [1–4].

Many studies have been carried out to improve one or more of the abovementioned parameters or to provide different circuit techniques to improve the overall performance of the whole comparator circuit [5–10]. However, due to the disadvantages of the conventional dynamic comparators including: high delay, high dynamic power consumption and input-referred voltage errors; the designers have led to the development of the modified double-tail dynamic comparators [5]. However, in order to improve the speed/accuracy trade-off of low-power ADCs, the improvement in the speed performance and power consumption of the double-tail dynamic comparators has drawn the most attention of the analogue integrated circuits designers [11–15]. In the recent years, various approaches have been discussed in [16–23], to improve the input offset performance of the comparators. Moreover, the reduction of the input-referred noise has been addressed in [24, 25].

In [1, 8–14] and [26–28], the positive feedback circuit has been added to the core body of the pre-amplifier stage to significantly reduce the comparator response time (delay). However, the positive feedback circuit itself increases both the power consumption as well as the input-referred noise [1]. For example, in [1], two transistors are utilised in series with the input differential pair as control switches in the pre-amplifier stage, to control the power consumption of the circuit. However, a larger chip area, incapability to operate in low supply voltages, and high input-referred noise due to the use of positive feedback block in the pre-amplifier stage, are the major disadvantages of the designs reported in [1, 8–14]. On the other hand, realising the integrated circuits in the sub-threshold region and bulk-drive techniques are the main two approaches that significantly reduce the power consumption, while increase in the delay of the circuit can be considered as a reduction in the speed performance. In addition, the supply boosting approach is another technique that is used in the realisation of low-voltage circuits [13].

However, the mismatch existence between the transistors and the offset voltage error are two other important issues in the comparator design in the nanometre technologies. For negligible mismatch effects, larger transistors have to be selected; this increases the parasitic capacitances and leads to the slower charging and discharging of the capacitors. Moreover, larger transistor dimensions themselves increase the transconductance of the transistor, which results in a faster speed for the comparators. Therefore, the delay time decreases, while the dynamic power consumption increases with larger capacitances, and the circuit occupies a large chip area. Although the dynamic power consumption is significantly reduced by the lower supply voltage, the reduction in drain currents of the transistors increases the delay of the comparator. On the other hand, the deep sub-micron technologies suffer from high leakage currents, which leads to a higher leakage power consumption [29]. Furthermore, in these technologies, the threshold voltage is not reduced accordingly with the supply voltage reduction, so the reductions in supply voltage and power consumption may result in serious design challenges. These challenges have attracted the designers' attention to other emerging technologies [30]. An alternative to the conventional CMOS technology is the Carbon Nanotube Field Effect Transistor (CNTFET) technology. Therefore, the proposed comparator in this paper is designed in CNTFET technology.

It is worth mentioning that, unlike previous designs, only four transistors are added to a conventional double-tail comparator circuit to automatically control the threshold voltage of the inverters utilised in the proposed latch stage. As a result, the delay of the proposed comparator is reduced without imposing extra values of power consumption. The reduced delay value allows the proposed comparator to operate in high-speed applications up to 15 GHz, with a low power consumption in the scale of micro-watt (μW).

This paper is organised as follows: In Section 2, the physical and electrical characteristics of the CNTFET technology are introduced. The performance of the conventional double-tail dynamic comparators and some previously reported comparator designs are reviewed in Section 3. In Section 4, the proposed comparator circuit is discussed in detail. Section 5 presents the simulation results of the proposed circuit in CNTFET technology. Finally, Section 6 compares the simulation results with other previously reported designs and presents the concluding remarks.

2 | A BRIEF REVIEW ON CARBON NANOTUBE FIELD EFFECT TRANSISTOR TECHNOLOGY

CNTFETs have an improved off-state leakage current compared to the conventional MOSFET transistors in CMOS technology [31]. Therefore, a larger ratio of on-state current to off-state leakage current (I_{ON}/I_{OFF}) can be obtained for the CNTFET devices [31–33]. Moreover, other advantages of CNTFETs, such as: ballistic transport of the carriers in low supply voltage, low power consumption and very small dimensions, enable CNTFETs to be considered as a proper alternative for replacing the CMOS technology in emerging high performance and high-density chips. These transistors can also exhibit ballistic transport of charge carriers between the source and drain terminals at higher speeds [34–37]. In other words, CNTFETs can have the similar physical structure as the MOSFETs, but with the only difference that in CNTFET the carbon nanotubes (CNT) between the drain and source terminals act as the conducting channels [38].

Nanotubes are formed by rolling up a graphene sheet along a vector which is called "chiral vector (n_1, n_2)" as shown in Figure 1. If $(n_1 - n_2) \neq 3k$, (where k is assumed as an integer

number), the nanotube acts as a semiconductor. Otherwise, CNT acts as a metal [31–33].

In addition, the nanotube diameter can be calculated based on the Equation (1):

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \quad (1)$$

where, a is the lattice constant, which is equal to 2.49 Å.

The width of the CNT transistor can be calculated using Equation (2) as follows,

$$W_{gate} = MAX\,(W_{min}, (N-1)Pitch + D_{CNT}) \quad (2)$$

where, W_{min} is the minimum gate width, N is the number of nanotubes, pitch is the distance between the two adjacent nanotube centres, and DCNT is the nanotube diameter [31, 32].

As reported in [38], the major advantage of the CNTFETs is their threshold voltage tunability. The threshold voltage of a CNTFET is inversely related to the diameter of the nanotube as it is given in Equation (3).

$$V_{TH} \approx \frac{E_g}{2e} \approx \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \approx \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \approx \frac{5.5}{\sqrt{n_1^2 + n_1 n_2 + n_2^2}} \quad (3)$$

where, e is an electron charge, α is the scattering coefficient, V_π (= 3.033 eV) is the carbon π–π bond energy, and , E_g is the bond energy, which is inversely related to the nanotube diameter [31–33]. Obviously, by increasing the values of the chiral vector, the threshold voltage of the transistor decreases according to Equation (3).

3 | REVIEW ON THE DOUBLE-TAIL DYNAMIC COMPARATORS

This section introduces some of the recent double-tail dynamic comparators while also reviewing their pros and cons. In subsection 3.1, a conventional double-tail dynamic comparator circuit is introduced, while subsections 3.2, presents the detailed descriptions of the recent reported designs discussed in [1], [11], and [26].

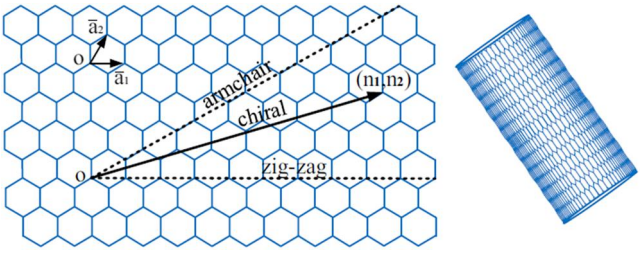

FIGURE 1 Graphene sheet and carbon nanotube basic structure [31]

3.1 | Conventional double-tail dynamic comparator circuit

Figure 2, shows the two stages of the dynamic comparator circuit, which include the pre-amplifier stage (input differential pair M1 and M2, the load transistors M3 and M4, and the current source Mtail1) and latch stage (two back-to-back inverters M7-M8 and M9-M10 and a tail transistor Mtail2). Transistors MR1 and MR2 are used to discharge the output nodes in the reset phase. Moreover, the presence of MR1 and MR2 between the internal nodes (fn and fp) and the main outputs, reduces the kickback noise. The circuit performance is as follows:

- Pre-charge or Reset phase For CLK = 0, both the tail transistors Mtail1 and Mtail2 are off. However, M3 and M4 are on and pre-charge the fn and fp nodes through the parasitic capacitors seen at these nodes up to the supply voltage of VDD. Therefore, MR1 and MR2 are turned on to discharge the output nodes Outn and Outp to GND.
- Decision or Comparison phase For CLK = 1, both the tail transistors Mtail1 and Mtail2 are on, while M3 and M4 are off. When Mtail1 is turned on, the capacitors at fn and fp nodes discharge with different speeds (depending on whether V_{INP} or V_{INN} is greater). For the case that V_{INP} greater than V_{INN}, fn is discharged faster than fp. Therefore, MR2 turns off faster than MR1.

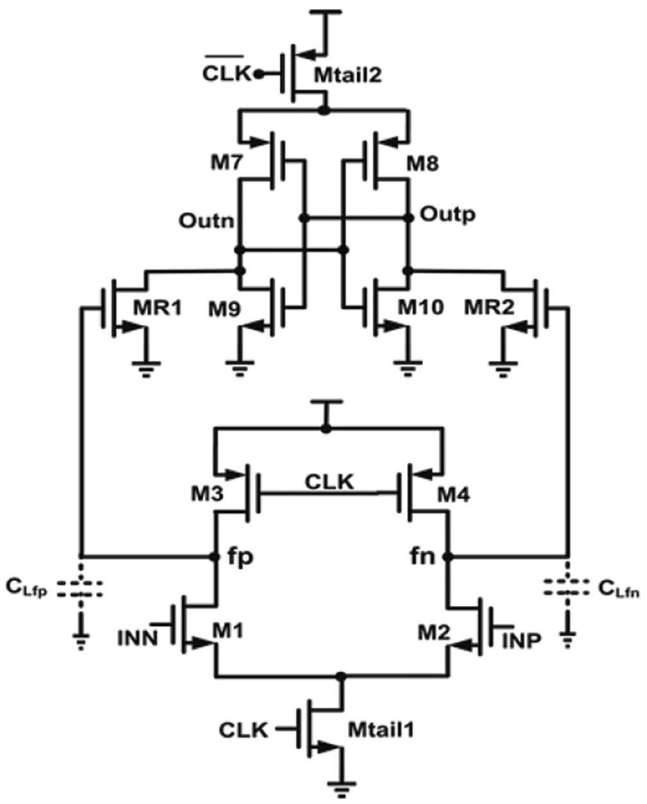

FIGURE 2 The conventional double-tail dynamic comparator [1]

When MR2 turns off, the voltage at Outp increases, while the load capacitor C_L is charged through M8. When the load capacitor of Outp is charged to the threshold voltage, the NMOS transistor of the opposite inverter, that is, M9, turns on and discharges the node Outn to GND. The delay of the comparator circuit is directly related to the value of the load capacitance, while it is inversely related to the differential input voltage (ΔVin), Itail2, common-mode input voltage, and the transconductances of MR1 and MR2 transistors. However, the main drawback of the conventional double-tail dynamic comparator is the high static power consumption due to the presence of MR1 and MR2 in the decision phase [1].

3.2 | Recently reported double-tail dynamic comparator designs

In a conventional double-tail dynamic comparator circuit, the capacitors seen at the fn and fp nodes are fully discharged in the decision phase. Therefore, fn and fp are pre-charged to the supply voltage during the reset phase which leads to a higher energy consumption during each conversion. The circuit presented in [1], besides with higher operating speed, has a lower power consumption due to the prevention of discharge in the internal nodes. The use of positive feedback in the pre-amplifier circuit increases the pre-amplifier speed which decreases the delay of the comparator. However, this considerably increases the kickback noise compared to the conventional dynamic comparator structure. The structure proposed in [1] still consumes static power due to the existence of path between the power supply and the ground (GND) through MR1 and MR2 and pull-up transistors in the latch stage. Moreover, in the decision phase for the circuit discussed in [1], the presence of the positive feedback transistors in the pre-amplifier circuit along with the differential pair and Mtail1 create a direct path between the power supply and ground, so the energy consumption of the comparator increases. To mitigate this drawback, switch transistors ($Msw_{1,2}$) are added to the pre-amplifier stage to cut the static current path in the decision phase.

In the pre-amplifier stage of the design discussed in [11], the voltage variation range is limited to $V_{DD}/2$ in order to reach the low power performance for the comparator. Besides, in this circuit, the input common-mode voltage level in the latch stage is increased to $V_{DD}/2$, in order to meet a faster speed performance in this stage. Therefore, a higher speed is achieved in this comparator compared to the conventional double-tail dynamic comparator. In the reset phase, the output voltage of the pre-amplifier stage is pre-charged to $V_{DD}/2$. This value can activate the second stage, leading to a static power consumption in the circuit. The voltage swing of the pre-amplifier stage is limited, so the power consumption of the circuit is considerably reduced (by a factor of 50%). Moreover, by using this approach, the time required to charge the output nodes of the pre-amplifier stage to the threshold voltage of the NMOS transistors in the latch stage is reduced, so, the circuit delay decreases and the speed of the comparator increases. Although the technique used in this circuit is efficient, the proper operation of the latch stage in the recent deep sub-micron technologies with a supply voltage of less than 1 V faces many severe challenges due to the stack limitations of four transistors in this stage. Moreover, this design has a high kickback noise compared to other designs, because of the considerable capacitance values located between the output and input nodes.

In [26], a hybrid double-tail comparator is proposed to reach the high-speed and low-power performances. Similar to the structure discussed in [1], the pre-amplifier stage includes a positive feedback structure. But, the latch structure is formed by eliminating the tail transistors and reset transistors (MR1, and MR2) and substituting them with two transistors, which are controlled by the output nodes of the pre-amplifier. The structure proposed in [26], has a high operation speed due to the positive feedback in the pre-amplifier stage, but, it has a higher power consumption compared to the conventional double-tail dynamic comparator. Additionally, the positive feedback in the pre-amplifier stage results in a high kickback noise compared to the conventional double-tail structure.

4 | THE PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

In the proposed circuit presented in this paper, the decision speed is enhanced by utilising only four transistors in the latch circuit of a conventional double-tail dynamic comparator structure. Moreover, the use of CNTFETs enables the designer to reduce the delay in turning on M9 (M10) by adjusting the threshold voltage of the transistors in the double-tail dynamic comparators (Figure 2). Figure 3, illustrates the overall design of the proposed circuit in which M3 and M4 are added to a basic inverter structure and their drain terminals are connected to the body terminals of M1 and M2, respectively.

The performance of the proposed circuit is as follows:

- When the input signal (fp) increases, V_{OUTn} decreases while V_{DD}-V_{OUTn} increases, and for V_{DD}-$V_{OUTn} \geq |V_{TH3}|$, M3 turns on. Therefore, $V_{SB1} = -V_{DD}$; moreover,

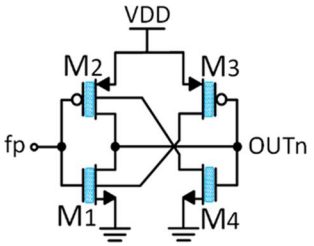

FIGURE 3 The proposed basic automatic threshold voltage control structure

from Figure 4, the threshold voltage of M1 for chiral vector (19, 0) decreases by 25% compared to that in V_{th0}. Consequently, the output of the inverter has a faster pull-down process time. Besides the abovementioned approach, as mentioned in Section 2, a proper chiral vector should be selected for the inverter transistors to reduce their threshold voltage and enhance the decision speed.

Figure 5, shows the proposed circuit in which the comparator delay time is reduced using the concept of the automatic threshold voltage control. The pre-amplifier stage consists of M1-M4 and the tail transistor (Mtail1). Moreover, M7-M10 are forming the two back-to-back inverters. Transistors M11-M14 are the switches which activate the speed-up circuit that can automatically shift the voltage transfer characteristic (VTC) of the inverters to the left or right. Transistors MR1 and MR2 separate the pre-amplifier stage from the latch stage to effectively reduce the kickback noise.

Considering the speed of the comparator, the operation of the circuit can be explained as follows: If the input V_{INp} is greater than V_{INn} in the pre-amplifier circuit, the voltage at

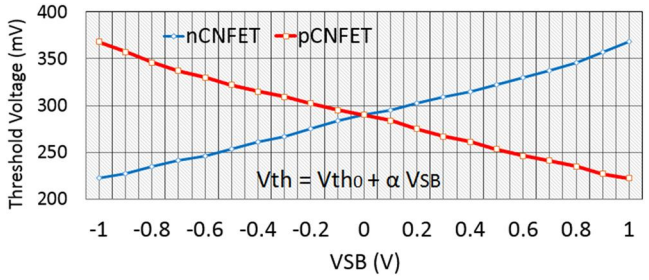

FIGURE 4 Threshold voltage variations of the Carbon Nanotube Field Effect Transistor (CNTFET) versus V_{SB}

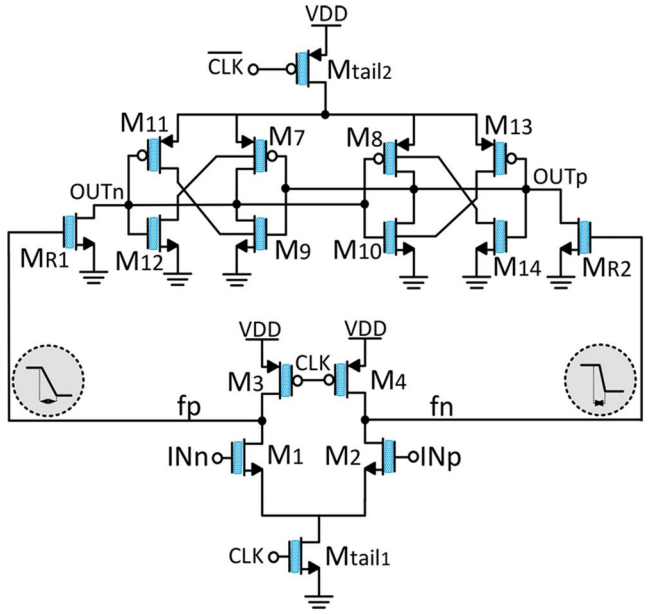

FIGURE 5 The proposed speed boosting approach employed in the proposed comparator

fn node discharges faster, and if fn voltage becomes less than the threshold voltage of MR2, then MR2 turns off. Then, V_{OUTp} charges faster up to the threshold voltage of M9, which turns on and pulls V_{OUTn} down towards GND. Meanwhile, V_{OUTn} discharges to V_{DD}-$V_{OUTn} \geq V_{TH11}$, that is, M11 turns on and the source-bulk voltage of M9 becomes $-V_{DD}$ to reduce its threshold voltage. Therefore, M9 pulls V_{OUTn} down faster than the conventional comparator circuits. Moreover, by increasing V_{OUTp} voltage level, M14 turns on and the source-bulk voltage of M8 becomes V_{DD}. This reduces the threshold voltage of M8, while V_{OUTp} charges to "1" logic faster.

The overall power consumption of the circuit can be expressed as Equation (4). In this equation, P_{pre} is the dynamic power which is consumed by the pre-charging process at fn and fp nodes, P_{latch} is the power consumed by the back-to-back inverters of the latch stage, and P_{trans} is the power consumption during the transition from the reset phase to the decision phase.

$$P_{diss} = P_{pre} + P_{latch} + P_{trans} \tag{4}$$

Due to the fact that the leakage current in CNTFET technology is very low [32, 33], the leakage power of transistors in the pre-amplifier stage in decision phase can be ignored, and P_{pre} can be obtained using Equation (5). In this equation, f_{clk} is the comparator clock frequency, R_{on3} (R_{on4}) are the on-state resistances of M3 (M4), respectively, and C_{fn} (C_{fp}) are the parasitic capacitances of the internal nodes.

$$\begin{aligned} P_{pre} &= \frac{1}{T}\int_0^{\frac{T}{2}} V_{DD}\, I_{supply}\, dt = f_{clk}\, V_{DD} \int_0^{\frac{1}{2f_{clk}}} I_{Cfn(fp)}\, dt \\ &= \frac{f_{clk}\, {V_{DD}}^2}{R_{on3(4)}} \int_0^{\frac{1}{2f_{clk}}} e^{\frac{-t}{R_{on3(4)} C_{fn(fp)}}}\, dt \end{aligned} \tag{5}$$

It is worth mentioning that the proposed latch circuit consumes the power mainly in the decision phase. At the beginning of the decision phase, M7 and M8 are on. Assuming that V_{INp} is greater than V_{INn}, at the end of t_0, M9 turns on, and since M7 is turned on, the latch regeneration initiates and power is consumed due to the activation of the inverter (transistor pair M7 and M9). This power is consumed until t_p (i.e., when M7 turns off). After t_p, M7 turns off, and the current flows from the power supply corresponds only to M8. Considering the above facts and ignoring the leakage current of the transistors, the power consumption of the latch stage can be expressed as Equation (6).

$$\begin{aligned} P_{latch} &\approx f_{clk}\, V_{DD} \int_{\frac{T}{2}}^{T} (I_{M7} + I_{M8})\, dt \\ &\approx f_{clk}\, V_{DD} \left[\int_{\frac{T}{2}}^{t_0} I_{M7}\, dt + \int_{t_0}^{t_p} I_{inv7,9}\, dt + \int_{\frac{T}{2}}^{T} I_{M8}\, dt \right] \end{aligned} \tag{6}$$

Since, in the VTC curve of the inverter, the time for changing the inverter state (t_p-t_0) is considered to be very short, the second term in Equation (6) can be ignored and after some mathematical simplifications the latch power consumption can be expressed as Equation (7).

$$P_{latch} \approx f_{clk}\, V_{DD} \left[\int_{\frac{T}{2}}^{t_0} C_L \frac{dV_{outn}}{dt}\, dt + \int_{\frac{T}{2}}^{T} C_L \frac{dV_{outp}}{dt}\, dt \right] \approx f_{clk}\, V_{DD} C_L \left[V_{th_{10}} + VDD \right] \tag{7}$$

As it is mentioned in the previous section, the tail transistor of the latch turns ON from the beginning of the decision phase until the voltage level of the fn (fp) nodes are greater than the threshold voltage value of MR1 (MR2), that is, during t_0. However, this has no significant effect on the performance of the latch stage, and only increases the power consumption. Therefore, the power for the transition from reset phase to decision phase, which results from the current shown in Figure 6, can be calculated as it is expressed in Equation (8).

$$P_{trans} \approx f_{clk}\, V_{DD} \int_{t_{ON-tail2}}^{t_0} (I_{tail2})\, dt \approx f_{clk}\, V_{DD} I_{tail2} \left(\frac{2C_L V_{th_{9(10)}}}{Itail_2} - t_{ON-tail2} \right) \tag{8}$$

In fact, to reduce the transition dynamic power, Mtail2 must be turned on after turning MR1 (MR2) off, which means that the terms in the above parenthesis at the right side of Equation (8), are approximately zero.

Giving the above facts, the final circuit structure of the proposed comparator is shown in Figure 7. In this structure, Mtail2 (see Figure 6) is substituted by two parallel transistors, Mtail2p and Mtail2n, which are controlled by the voltages at the nodes of fp and fn, respectively. Therefore, the leakage current path during the mentioned transition is cut and the energy per conversion (EPC) is reduced effectively. In designing Mtail2p and Mtail2n, the proper sizing of these transistors is very important, since they have to use a current with the value of half of the drain current of Mtail2, once they turn on. In addition, by adjusting the threshold voltage of these transistors and MR1 and MR2, the EPC (i.e., the term P_{trans}) value can be controlled and reduced effectively. Note that in this design adjusting the threshold voltage of transistors by varying the nanotube diameter can be considered as an advantage of employing the CNTFET technology.

The delay of the proposed comparator can be obtained using Equation (9).

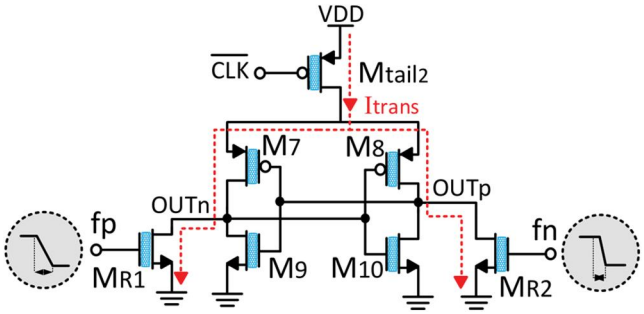

FIGURE 6 The current path through the latch stage during the transition time from reset to decision phases

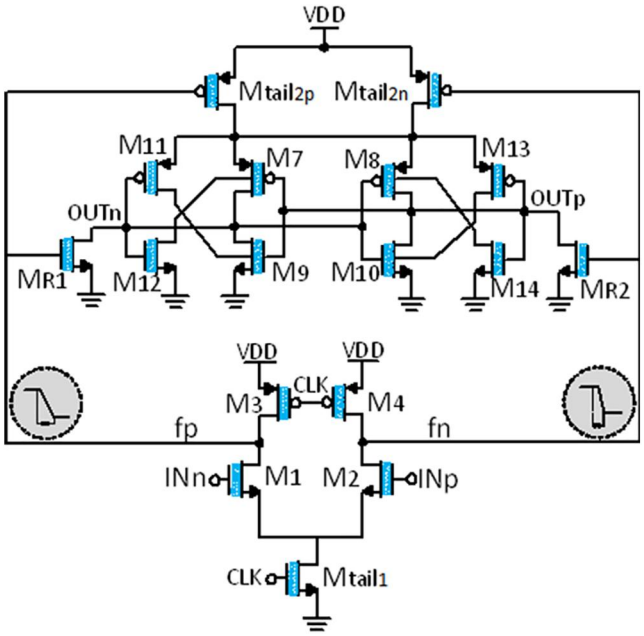

FIGURE 7 The complete proposed comparator circuit with improved speed and power performances

$$t_{delay} \approx \frac{2C_L V_{th_{9(10)}}}{(Itail_{2p} + Itail_{2n})} + \frac{C_L}{g_{meff}} \ln \left(\frac{V_{DD} (Itail_{2p} + Itail_{2n})^2 C_{L,fn(p)}}{8V^2_{thn}\, C_L g_{mR1,2}\, g_{m1,2} \Delta Vin} \right) \tag{9}$$

According to Equation (9), there is a direct relationship between the threshold voltage and the comparator delay parameter. So, the employment of the proposed automatic threshold voltage reduction technique in the decision phase, can effectively reduce the overall comparator delay. Moreover, special physical properties of the CNTFET technology, such as lower parasitic capacitances and higher transconductance efficiency, contribute greatly in the delay reduction of the proposed circuit.

5 | SIMULATION RESULTS

To evaluate the performances of the proposed circuit and compare them with the previously reported designs, the HSPICE circuit simulator and 32 nm Stanford CNTFET technology model parameters are employed. Moreover, in order to have a fair comparison, all of the considered previously reported designs as well as the proposed comparator circuit are simulated under the same simulation conditions in CNTFET technology such as the same supply voltage, input common-mode voltage (V_{CM}), differential input voltage (Δvin), and load capacitance. The size of the transistors in all the circuits are chosen so that they correctly operate with the highest sensitivity at their maximum operating frequency. Figure 8, shows the performance of the proposed comparator for V_{CM} = 0.7 V, Δvin = 0.3 mV, at the clock frequency of 12 GHz. According to the simulation results, the proposed circuit delay is obtained as 22.58 Psec, which confirms the performance of the proposed comparator for high-speed applications.

The simulation results of the proposed circuit are summarised in Table 1, where they are compared with other reported designs. In Table 1, a common-mode voltage of 0.7 V is selected for both the proposed comparator and the circuit reported in [1], since they both employ N-Type transistors as the input differential pair in their pre-amplifier stage. Moreover, a common-mode voltage of 0.3 V is applied for the structures reported in [11, 26], since they employ a P-Type transistor input differential pair in their pre-amplifier stage. Therefore, the conditions are considered the same for all the comparator circuits. Additionally, in order to perform a better multi objective comparison between the different circuit performances, a Figure Of Merit (FOM) is used based on the definition reported in [10], which is expressed in Equation (10).

$$\mathrm{FOM} = \frac{\mathrm{Fmax}}{\mathrm{Power}\ .\ \mathrm{Delay}} \tag{10}$$

According to the simulation results, the comparator proposed in [11] has the highest delay and the comparator proposed in [1] has the highest energy consumption value. Moreover, the comparator in [11], has the lowest FOM value, while the proposed comparator has the highest FOM. The simulation results show that the comparator in [1] shows 39% improvement in maximum speed than the conventional double-tail comparator [5], but both designs fail to operate properly at higher frequencies up to the frequency of the proposed circuit. It is worth mentioning that the performance improvement that has been reported in [1], was 33% in 180 nm CMOS technology. It is also noticeable that since the main objective of the proposed design is to increase the speed of the comparator, the improvement in the speed parameter for the proposed structure is obtained as 54% due to the use of the proposed speed-up technique and also benefiting from the CNTFET technology, which results in the higher efficiency for the proposed circuit in terms of the FOM parameter in comparison with other reported designs.

Furthermore, Figure 9, shows the performance of the proposed circuit at maximum speed, for V_{CM} = 0.7 V. As it is obvious, the accuracy performance of the proposed circuit can be verified at the clock frequency of 14.2 GHz with a resolution of 0.3 mV.

To compare the performance of the proposed circuit with other reported circuits, all the targeted circuit topologies

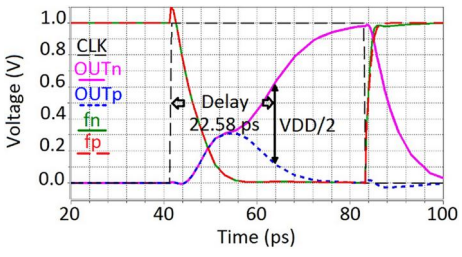

FIGURE 8 Transient simulation of the proposed comparator for Δvin = 0.3 mV, V_{CM} = 0.7 V, V_{DD} = 1 V and F_{CLK} = 12 GHz

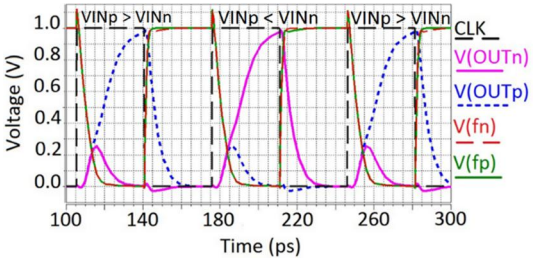

FIGURE 9 Transient simulation of the proposed comparator for VCM = 0.7 V and Δ*V*in = 0.3 mV at maximum clock frequency

TABLE 1 Performance comparison for different comparators in 32 nm Carbon Nanotube Field Effect Transistor (CNTFET) technology under the same simulation conditions (ΔVin = 0.3 mV and V_{DD} = 1 V)

Parameters	Conventional double-tail [5]	[1]	[11]	[26]	Proposed
F_{max} (GHz)	**9.2**[a]	12.8	10.5	9.6	14.2
Delay (ps)	25.9	19.6	**26.3**[a]	24.3	22.6
Power (μW)	25.75	**62.89**[a]	47.27	34.36	42.38
Energy/Conv. (aJ)	27.99	**48.13**[a]	45.02	35.79	29.85
FOM (F_{max}/Power×Delay)	1.38e+25	1.04 e+25	**0.84 e+25**[a]	1.15 e+25	1.48 e+25

[a]The worst-value for each parameter is bolded for more emphasis.

including the conventional double-tail and the circuits reported in [1, 11, 26] as well as the proposed comparator in this paper are simulated in CNTFET technology under the same simulation conditions, (F_{ClK} = 6 GHz, V_{DD} = 1 V, ΔVin = 0.3 mV and C_L = 5 fF). The simulation results are summarised in Table 2 and shown in Figure 10. The simulation results show that the comparator in [1] has only 17.9% less delay time, while it consumes 54.9% more power than the proposed circuit. The results for the both speed and power performances based on the FOM parameter comparison show that the proposed circuit benefits from 31.3% better overall performance over the comparator proposed in [1].

The reported comparator in [1] has lower delay than the other designs, but, it has a much higher kickback noise value due to the use of the positive feedback circuit in the preamplifier stage. To calculate the kickback noise, the method discussed in [24] is used (Figure 11). The input voltage error values due to the kickback noise in the reported designs are shown in Figure 12. The proposed comparator has the minimum input-referred noise. Accordingly, the input-referred voltage error at the clock frequency of 6 GHz and ΔVin = 0.3 mV, is obtained as approximately of 80 μV in the decision phase and is less than 5 mV in the reset phase.

Figure 13, shows the input error voltage due to the kickback noise in the decision phase in terms of different Thevenin Resistances (R_{th}) for different values of differential input voltage. Clearly, the input-referred voltage due to the kickback noise is directly related to the Thevenin resistance and Δ*V*in; for a constant Thevenin resistance, the value of the input-referred error increases linearly as Δ*V*in increases.

To evaluate the performance of the proposed comparator circuit, the values of delay, power consumption, and EPC of the proposed comparator are simulated in terms of supply voltage variations for different values of Δ*V*in (see Figures 14 and 15). As it is shown in Figure 14, by increasing the supply voltage from 0.8 to 1.8 V, the comparator's delay time varies

TABLE 2 Performance comparison of different comparator circuits implemented in Carbon Nanotube Field Effect Transistor (CNTFET) technology

Parameters	Conventional double-tail [5]	[1]	[11]	[26]	Proposed
VCM	0.7 V	0.7 V	0.3 V	0.3 V	0.7 V
Delay (ps)	27.3	19.38	26.51	24.37	22.85
Power (μW)	16.98	29.34	26.85	28.64	18.94
Energy/Conv (aJ)	28.31	48.90	44.76	47.73	31.58

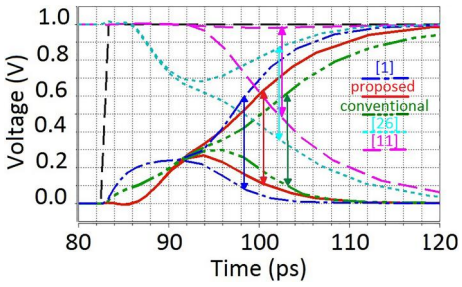

FIGURE 10 Delay simulation results comparison for (VCM = 0.7 V and Δ*V*in = 1 mV at 6 GHz)

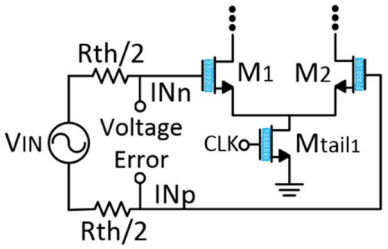

FIGURE 11 Measurement configuration for calculating the kickback noise

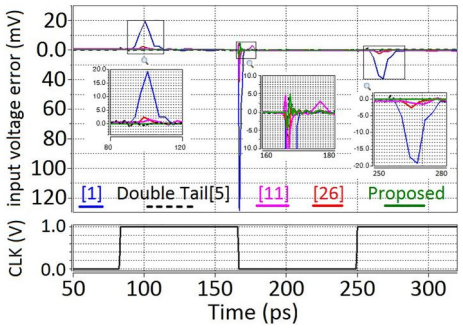

FIGURE 12 The input error voltage for the proposed circuit and other simulated designs due to the kickback noise at (Δ*V*in = 0.3 mV)

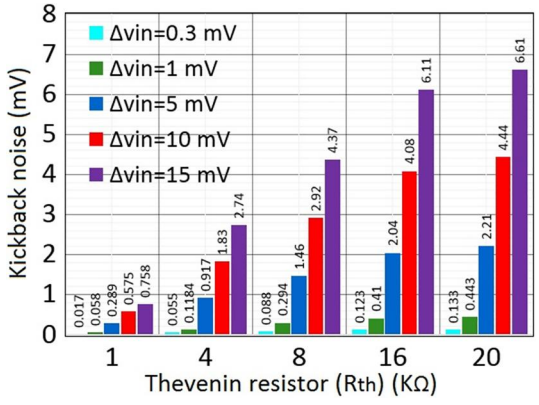

FIGURE 13 Input error voltage caused by the kickback noise versus R_{th} for different Δ*V*in

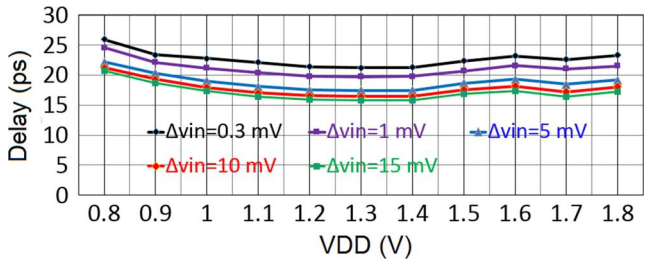

FIGURE 14 Delay versus V_{DD} variations (for different ΔVin) for the proposed comparator

less than approximately 5 psec. Moreover, this range of variations is almost the same for different values of ΔVin.

According to Figure 15a, by increasing the supply voltage from 0.8 to 1.8 V, the power consumption of the proposed comparator at ΔVin = 0.3 mV increases from 12.2 to 90.32 μW; this range decreases with increasing ΔV_{in}. Similarly, Figure 15b shows that for 1 V increase in the value of supply voltage (from 0.8 to 1.8 V), the obtained EPC (at ΔVin = 0.3 mV) increases from 4.06 to 30.10 fJ/conv, while at ΔVin = 15 mV, the range of EPC decreases to 21 fJ/conv.

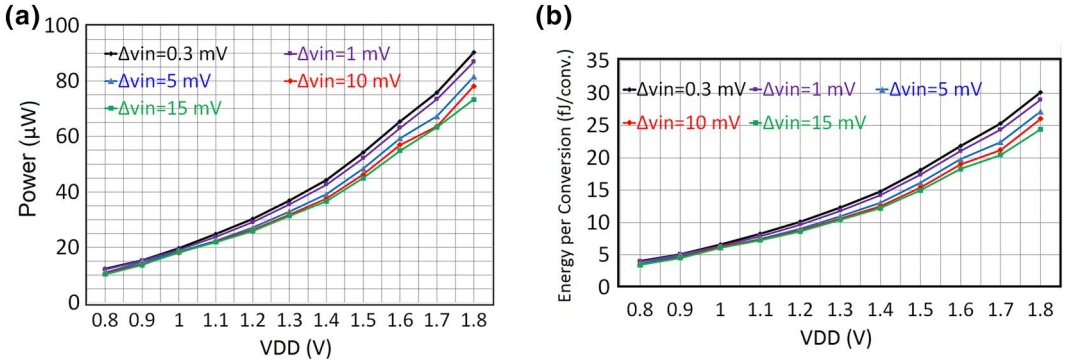

FIGURE 15 (a): Power consumption, (b): energy per conversion (EPC) performances, versus supply voltage (V_{DD}) for different ΔVin for the proposed comparator

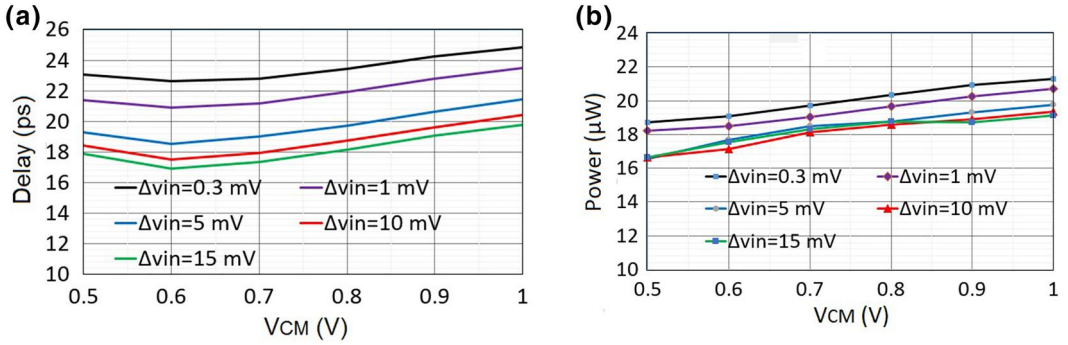

FIGURE 16 (a): Delay, (b): Power consumption performances versus V_{CM} for different ΔVin for the proposed comparator

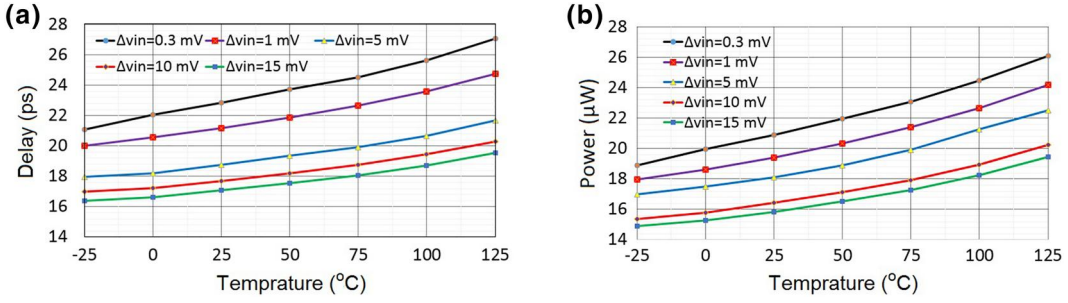

FIGURE 17 (a): Delay, (b): Power consumption performances versus temperature variations for different ΔVin for the proposed comparator

In order to investigate the performance of the proposed comparator circuit in terms of variations in the common-mode input voltage, V_{CM}, the values of the delay and power consumption parameters for different values of ΔVin are shown in Figure 16. According to Figure 16a, the delay slightly depends on the V_{CM} variations (less than 10%). Therefore, the proposed comparator can operate properly within a wide range of common-mode input voltage variations. Moreover, the simulation results in Figure 16b indicate that a 100% increase in the common-mode input voltage increases the power consumption by a maximum rate of 17%.

To investigate the temperature performance of the proposed comparator, the values of the delay and power consumption performances are simulated in the temperature range of −25 to 125°C and shown in Figure 17. It is worth mentioning that the rate of performance variations (slope) for delay and power consumption performance variations are obtained as of 1 ps/25°C and 1 μW/25°C, respectively.

Figure 18, shows the delay variations of the proposed comparator with respect to the changes in ΔVin at the supply voltage of 1 V. It is obvious that for ΔVin = 0.3 mV, the comparator delay is obtained as 22.81 Psec, and by increasing

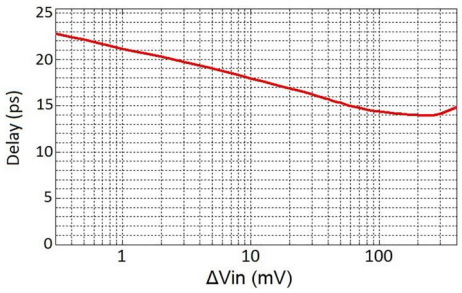

FIGURE 18 Delay versus Log (ΔVin) for the proposed comparator

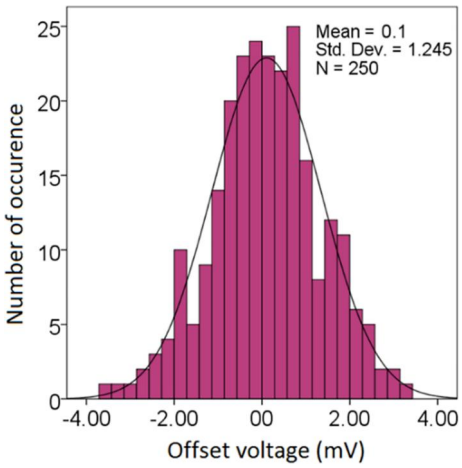

FIGURE 19 Monte-Carlo simulated histogram of the input offset voltage performance

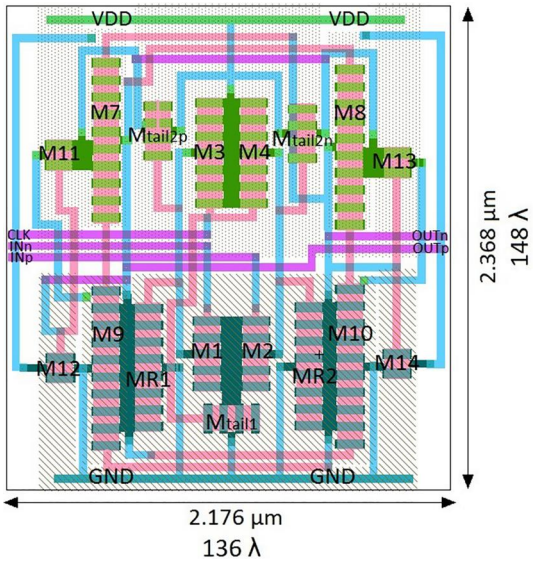

FIGURE 21 Layout view of the proposed comparator

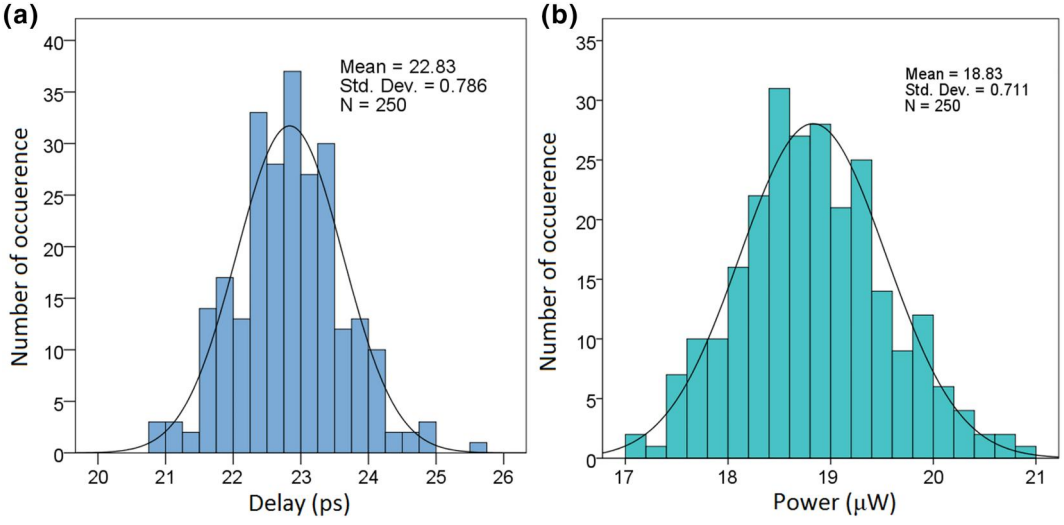

FIGURE 20 Monte-Carlo simulated histogram for (a): delay and (b): power consumption performances

TABLE 3 The performance comparison of the proposed circuit with other reported comparator designs

Parameters	[7]	[8]	[9]	[10]	[14]	[27]	This work
Year	2020	2020	2020	2019	2018	2019	2022
Supply power (V)	1.2	1	1	1	1	0.9	1
Power (μW)	106	>4.5	48.74	848	230	67	42.38
F_{max} (GHz)	4	0.025	19.6	6	0.5	6.25	14.2
Sensitivity (mV)	0.03	1	1	1	1	1	0.3
Delay @ F_{max} (pS)	190	13,000	40.71	36.6	>250	160	22.6
Input offset voltage (mV)	-	-	2.44	8	2	23	1.245
Area (μm^2)	57.8	1025	76.38	-	530	384	5.15
FOM (F_{max}/Power.Delay) (e+25)	0.019	-	0.987	0.019	-	0.058	1.48

the ΔVin, the comparator delay decreases with the rate at approximately 3.6 psec/dec.

Figures 19, 20a, and 20b, show the Monte-Carlo simulation results for 250 different runs for the offset voltage, delay, and power consumption parameters of the proposed circuit, respectively. The Mean and standard deviation values of the mentioned parameters are obtained based on the Monte-Carlo simulations for the changes of the design parameters (the pitch and the threshold voltage variations) of each CNTFET transistor. In the Monte-Carlo simulation, all mismatches are modelled as Gaussian distribution similar to the method reported in [33].

Based on the simulation results, the mean value of the offset voltage, delay, and power consumption are obtained as of 100 μV, 22.83 Psec, and 18.83 μW, respectively, while the standard deviation (1-σ) of the offset voltage, delay, and power consumption are obtained as: 1.245 mV, 0.786 Psec and 711 nW, respectively.

Furthermore, Figure 21 shows the layout area of the proposed comparator which successfully passed the DRC, LVS and ERC checks in the layout CAD tool [39]. As it is obvious in Figure 21, the proposed comparator circuit occupies a layout area of (148λ*136λ) in 32 nm CNTFET technology with (λ = 16 nm).

Finally, a complete comparison is done between the simulation results of the proposed comparator and other reported designs, as summarised in Table 3. The simulation results show the performance superiority of the proposed circuit over other reported designs. Based on the obtained FOM (expressed in Equation (10)), the proposed dynamic double-tail comparator shows approximately 50% better overall performance than the best reported design [9], and provides higher resolution, higher-speed, and lower-power consumption in a smaller chip size area, in comparison with other reported designs.

6 | CONCLUSIONS

In this paper, an energy-efficient dynamic comparator in CNTFET technology is reported which benefits from a circuit method that is introduced to improve the speed of the CNTFET-based dynamic comparator. In this approach, only four transistors were added to the comparator circuit which are acting as switches. The proposed method automatically controls the body voltage of the transistors in order to tune their threshold voltage to the proper values. In this method, by reducing the threshold voltage of the transistors that are considered as back-to-back inverter, the required time for turning on the transistors is decreased, which leads to the faster latch regeneration process. Moreover, two transistors, which are controlled by the pre-amplifier stage output, are used instead of the latch tail transistor to reduce the EPC. The performance and the accuracy of the proposed comparator circuit is simulated in HSPICE using 32 nm Stanford CNTFET model parameters at 1 V supply voltage. The simulation results showed that the proposed circuit can reduce the delay time up to 17%. In addition, according to the simulation results, the proposed circuit can properly compare the input signals with frequencies up to 14.2 GHz, while the conventional comparator circuit topology can compare the input signals with the frequencies of up to 9.2 GHz under the same simulation conditions, which justifies the good performance of the proposed circuit in comparison with other previously reported designs.

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this manuscript.

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