In The Name of Almighty

Lec. 8:
Subranging/Two-step ADCs

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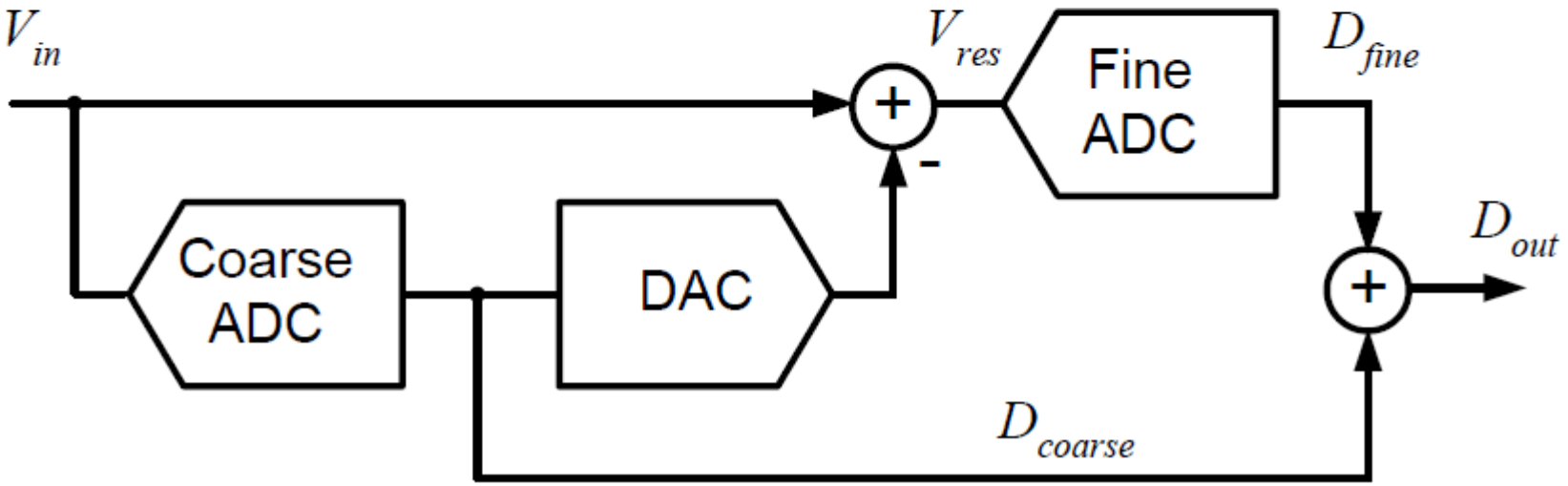
General Concept of Multi-Step Conversion

- General idea (two-step example)
  1. Perform a "coarse" quantization of the input
  2. Compute residuum (error) of step 1 conversion using a DAC and subtractor
  3. Digitize computed residuum using a second "fine" quantizer and digitally add to output



Subranging & Two-step Converters

- When the resolution is higher than 8-bit then instead of full-flash ADC, it can be more convenient to use a sub-ranging or a two-step algorithm for a better speed-accuracy trade-off.
- The **sub-ranging or the two-step implementation** require two (or three) clock periods to complete the conversion but they use a smaller number of comparators thus benefitting silicon area, power consumption and parasitic capacitance loading on the *S&H*.
- The architecture uses a sample-and-hold at the input to drive an *M-bit* flash-converter which estimates the *MSB*s (coarse conversion). The *DAC* then converts the *M-bits* back to an analog signal which is subtracted from the held input to give the coarse quantization error (also called the residue). Next, the residue is converted into digital by a second *N-bits* flash which yields the *LSB* (fine conversion). The digital logic combines coarse and fine results to obtain the *n=(M+N)-bit* output.
- **Sub-ranging**: without gain (No amplification of residue)
- **Two-step:** With amplifying the residue.

Sub-ranging/ Two-step

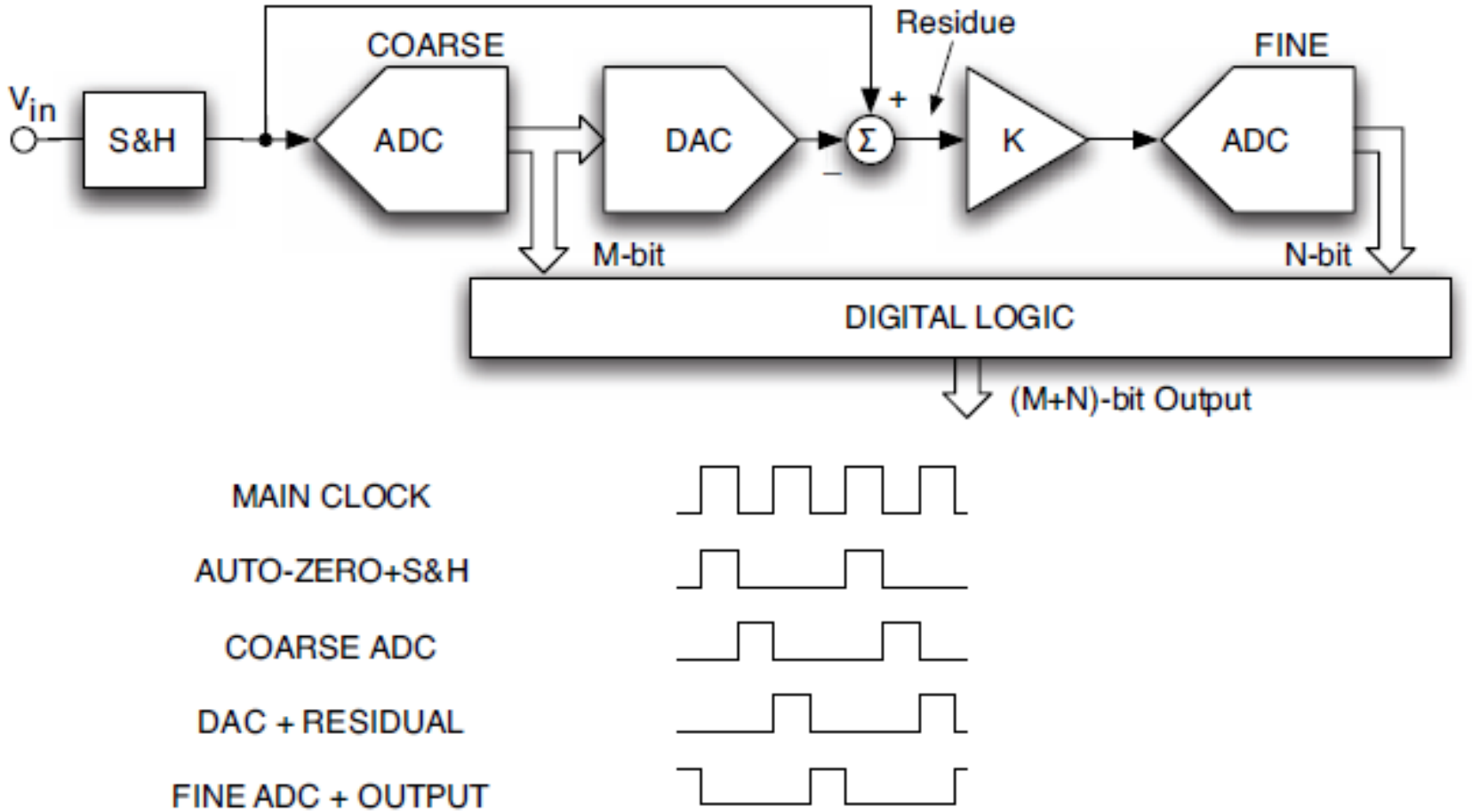
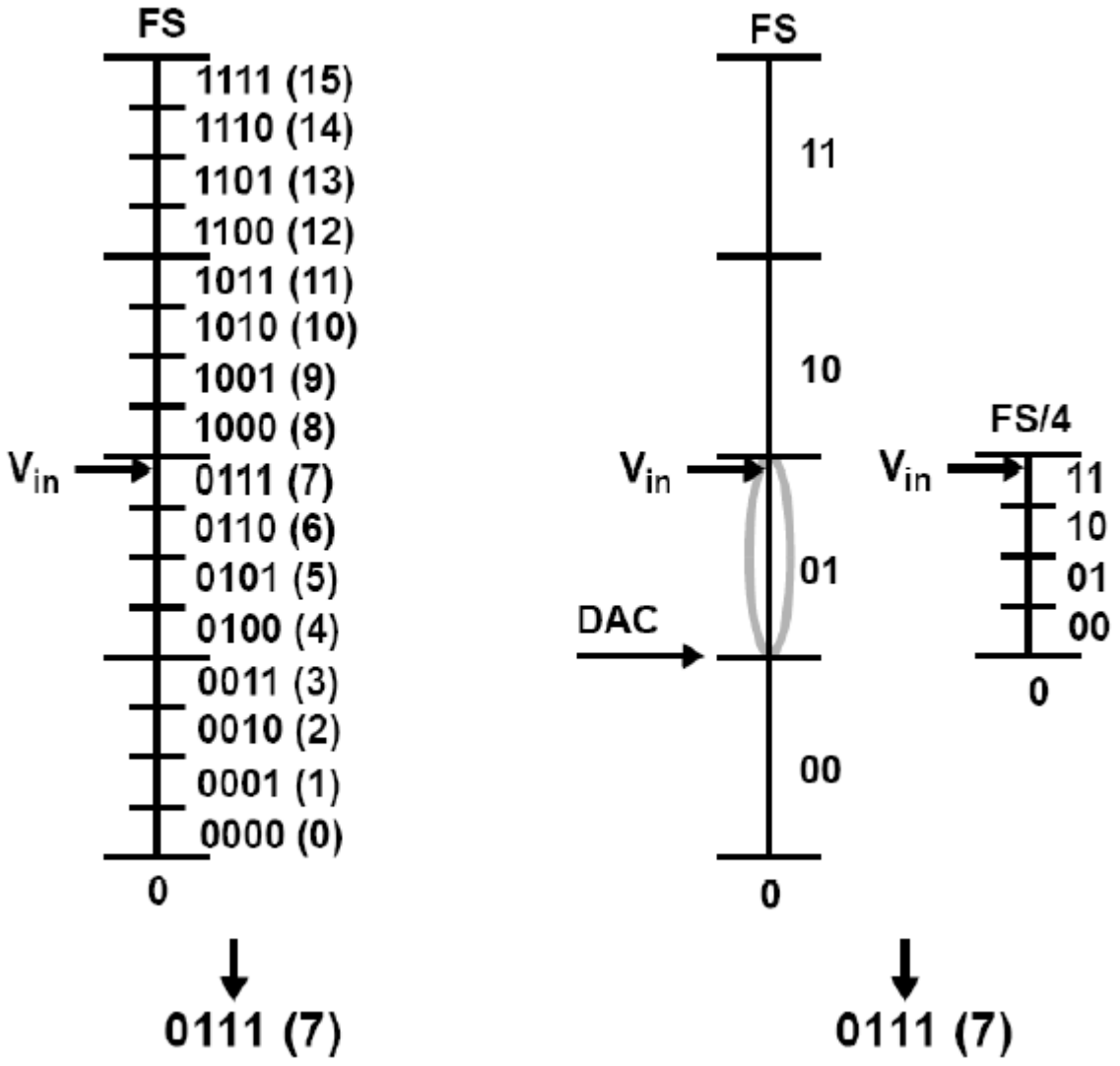


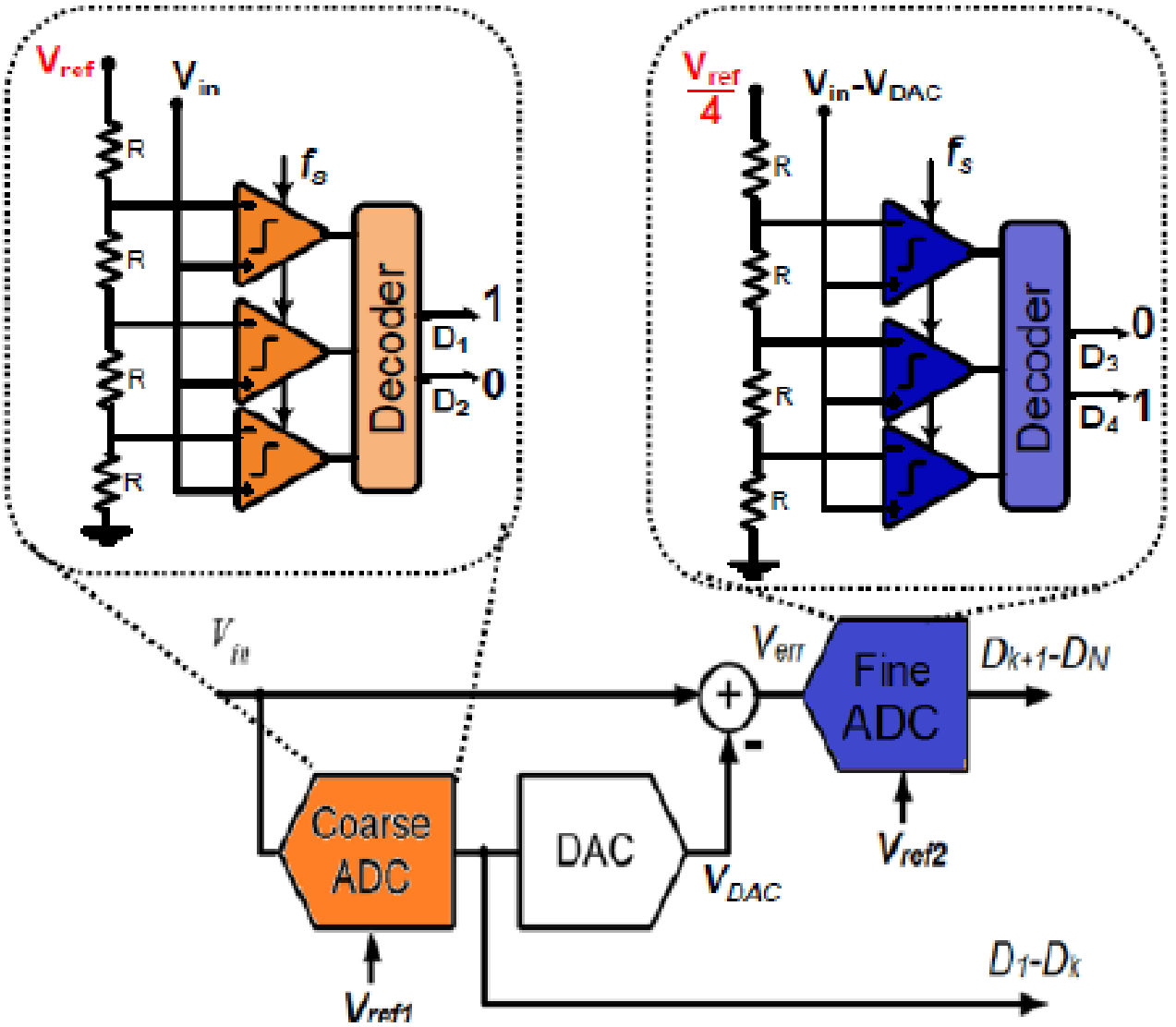
Figure 4.10. Block diagram of sub-ranging (K=1) and two-step architectures (K>1).

4-Bit Flash Vs. 4-Bit Two-Step ADC



Sub-ranging ADC

➢ Principal of Operation:



Pros/ Cons

- Pros:

✓ The Number of comparators is significantly reduced in compare with the full-flash ADC

- e.g. : for 8-bit (M=N=4), $2*(2^4-1)=30$ comparators are needed while for full-flash ($2^8-1=255$) comparators are needed.

✓ The spared area and power are much more than what is required to design the DAC and residue generator; moreover, the *S&H* is only loaded by 2^M comparators.

- Cons:

❖ Reduced conversion-rate as it is necessary to use two or three clock periods to complete the conversion. (But S/H is faster in sub-ranging due to the reduced parasitic input capacitance).

Delay of the Sub-ranging/Two-step ADC and possible Solution

- Conversion time :

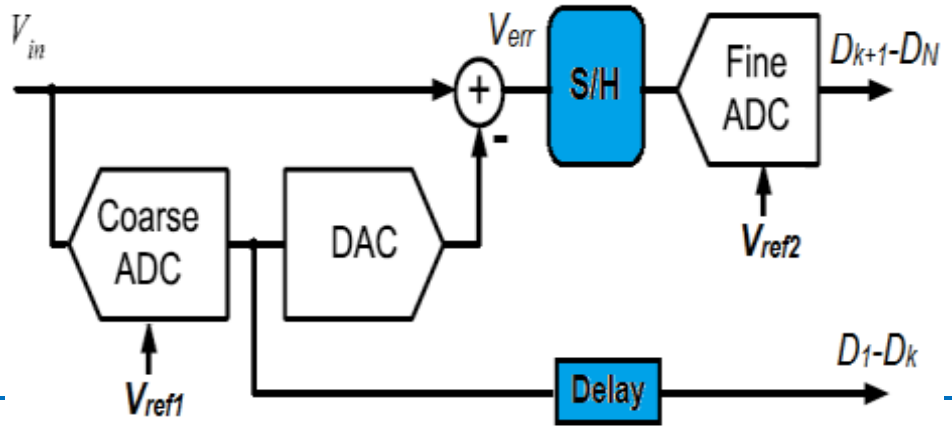
$$T_{conversion}=T_{course\text{-}ADC}+T_{DAC}+T_{subtractor}+T_{fine\_ADC}$$

- Solution:

Introduce a sample and hold operation after subtraction

→ During one clock cycle coarse & fine ADCs operate concurrently:

First stage samples/converts/generates residue of input signal sample # i While 2nd stage samples/converts residue associated with sample # i-1



The advantage of using Gain stage (A) in Two-step over sub_ranging

- Without amplifying the residue (without gain stage):

❖ The Fine ADC has to have precision in **the order of overall ADC 1/2LSB**

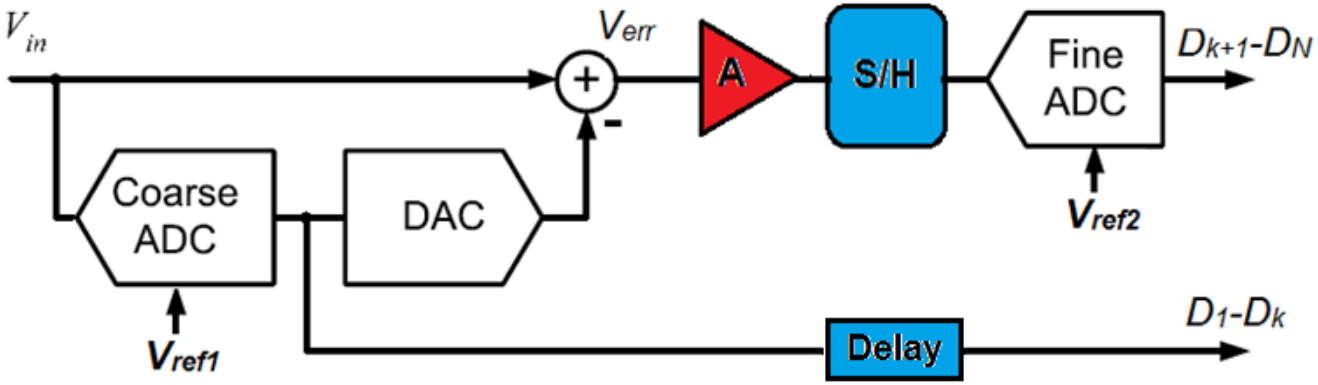
- E.g. 8 bit converter with 4-bit /4-bit partition; fine 4-bit decision levels must have "8-bit precision"

- **Solution:** Introduce Gain after Subtraction:

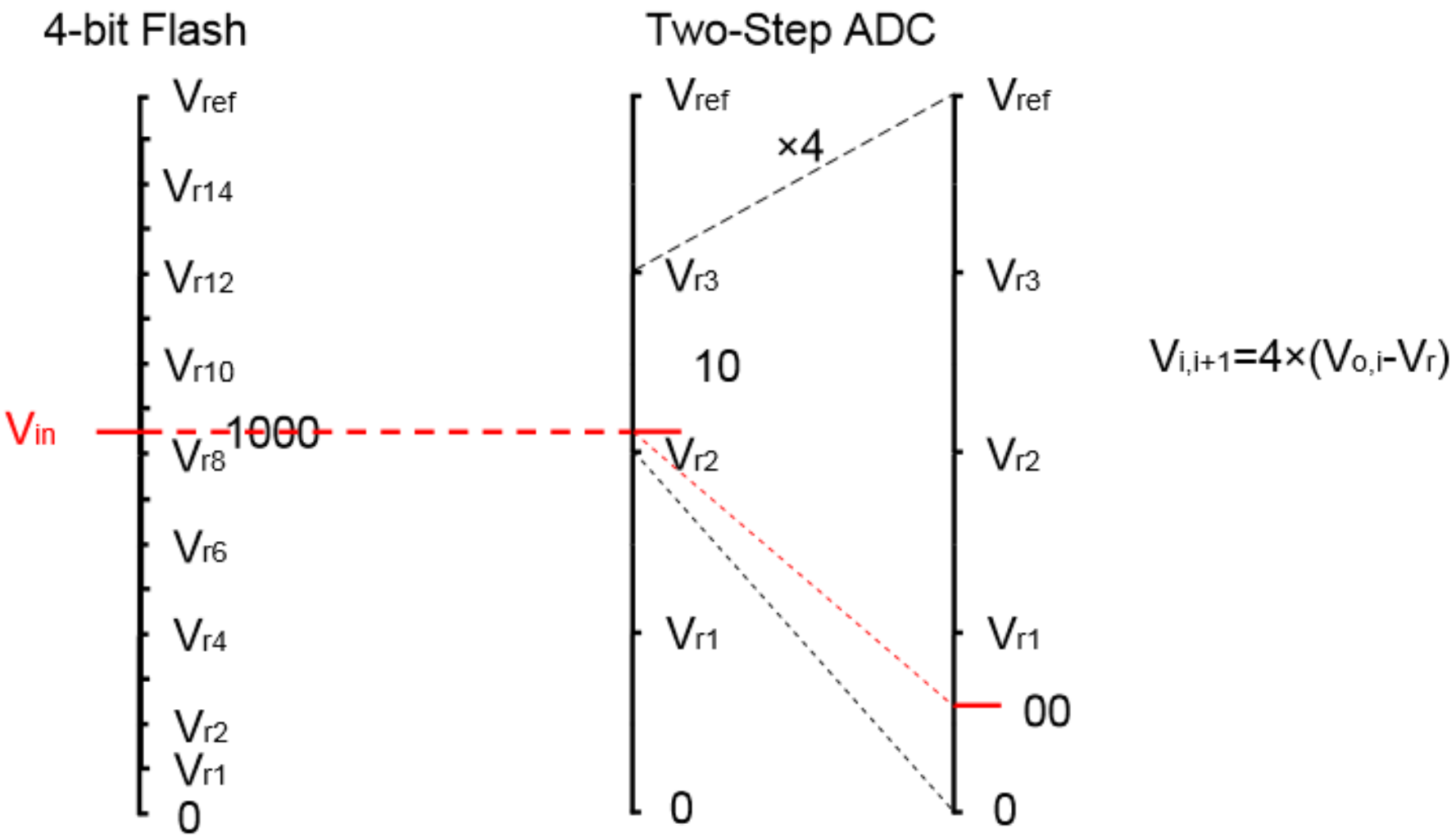
➢ Accuracy needed for fine ADC relaxed by introducing inter-stage gain

➢ All stages use a single Vref

➢ Advantageous for noise, matching and power dissipation

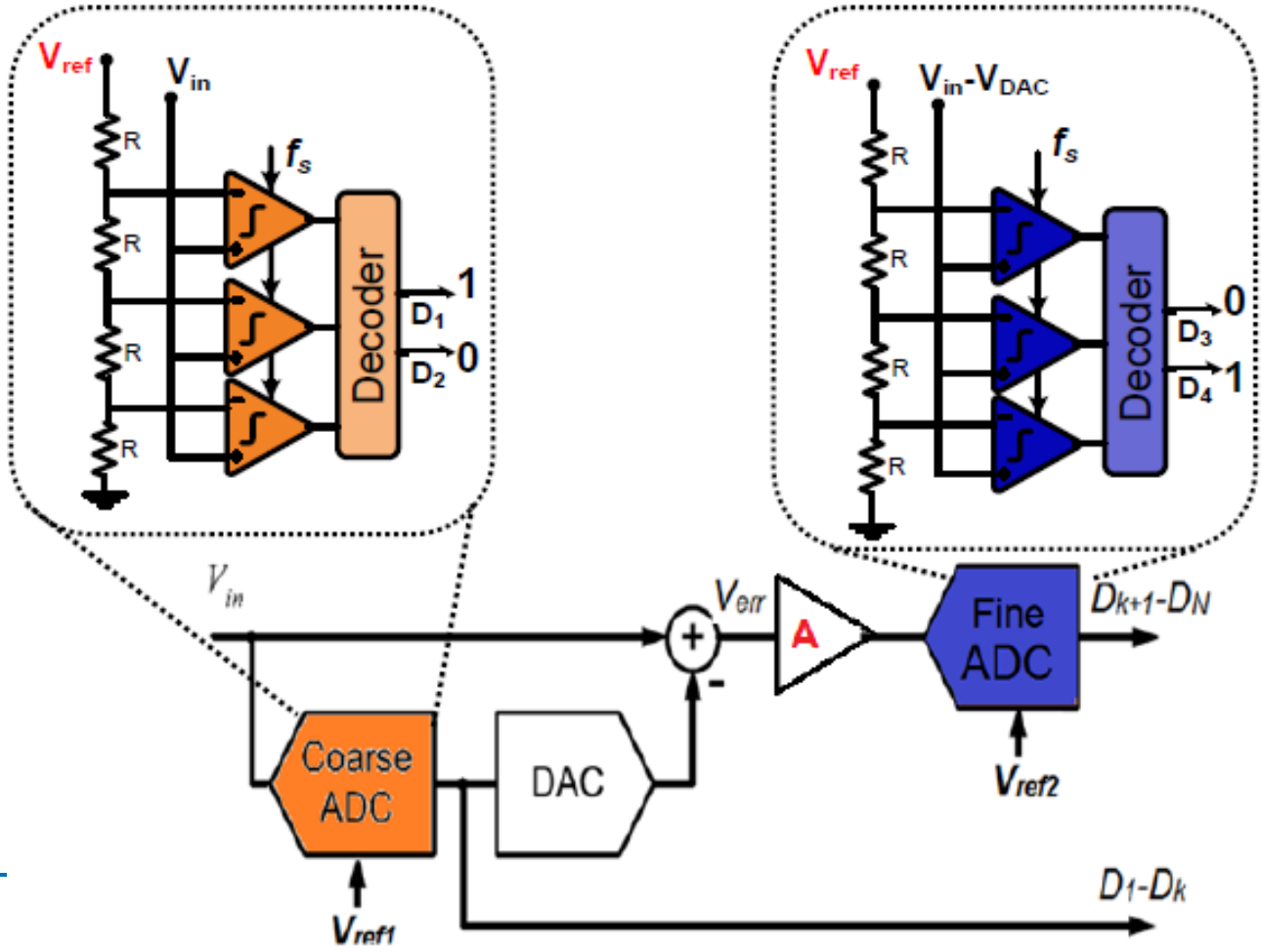


Quantization+Amplification

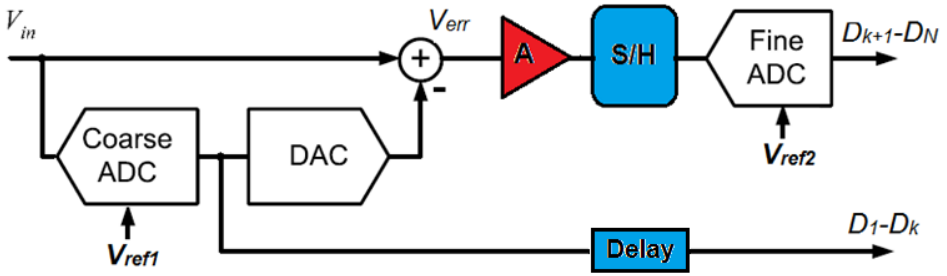


Two-Step principle of operation

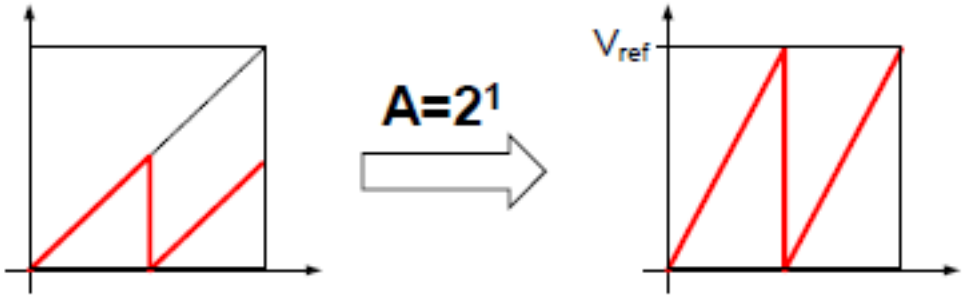
- Both course and fine ADC use V_{ref}. (in contrast to sub-Ranging i .e., V_{ref} for course and $V_{ref}/4$ for fine ADC-see slide 6)



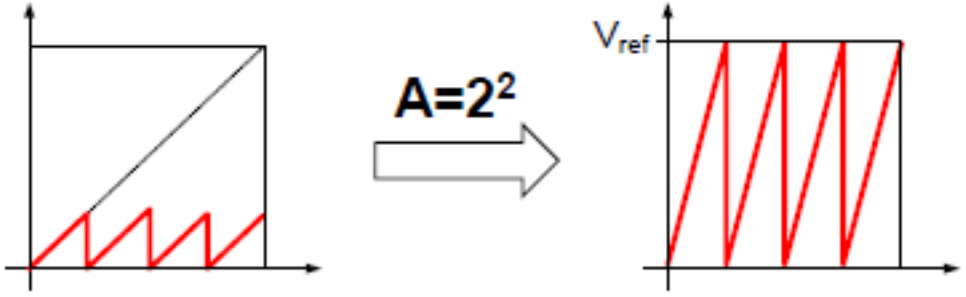
How Much gain?



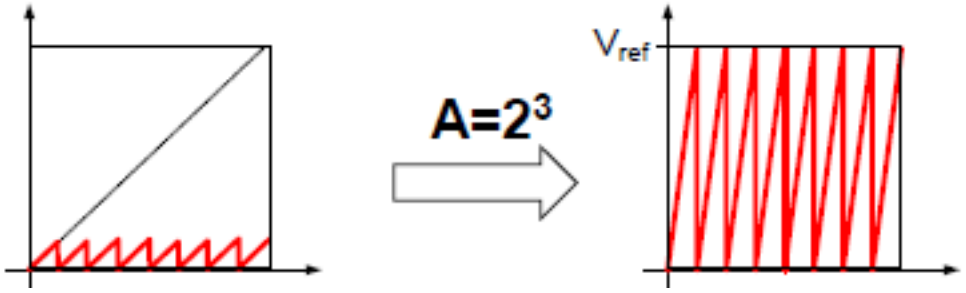
- For M=1 bit,



- For M=2 bits



- For M=3 bits



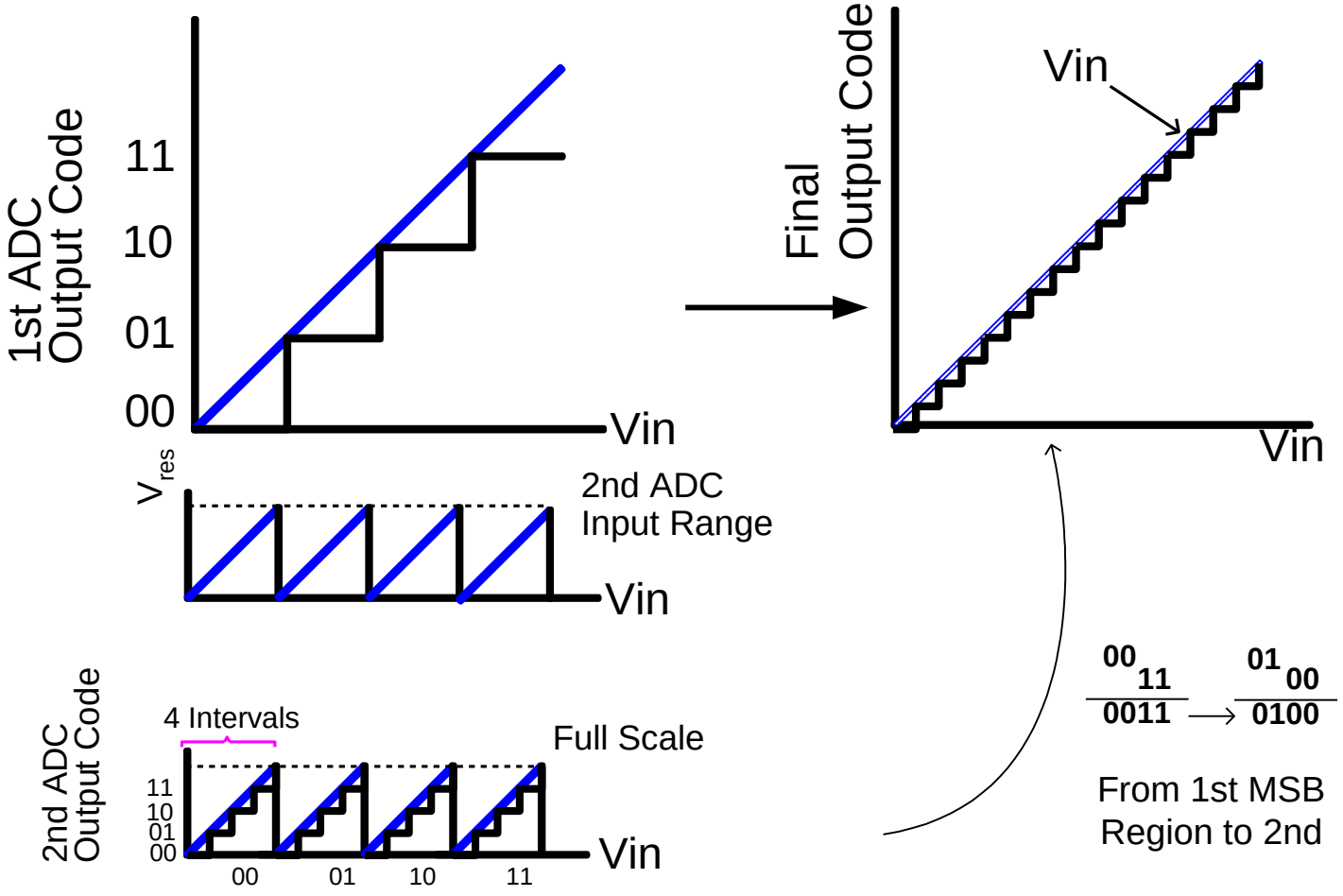
Accuracy Requirement

- Since the residue, determined by coarse *ADC*, *DAC* and gain factor *K*, is

$$V_{res}(V_{in}) = K\,[V_{in} - V_{DAC}(i)]$$
$$for: \quad V_{Coarse}(i-1) \leq V_{in} < V_{Coarse}(i);$$

- ideal *ADC* and *DAC* give rise to a residue that is a perfect sawtoothed non linear function of the input with amplitude confined between 0 and $VFS \cdot K/2^M$.
- However, limitations of the *ADC* and *DAC* cause errors on the break points and amplitude of the sawtooth.

Two-Step ADC – Ideal



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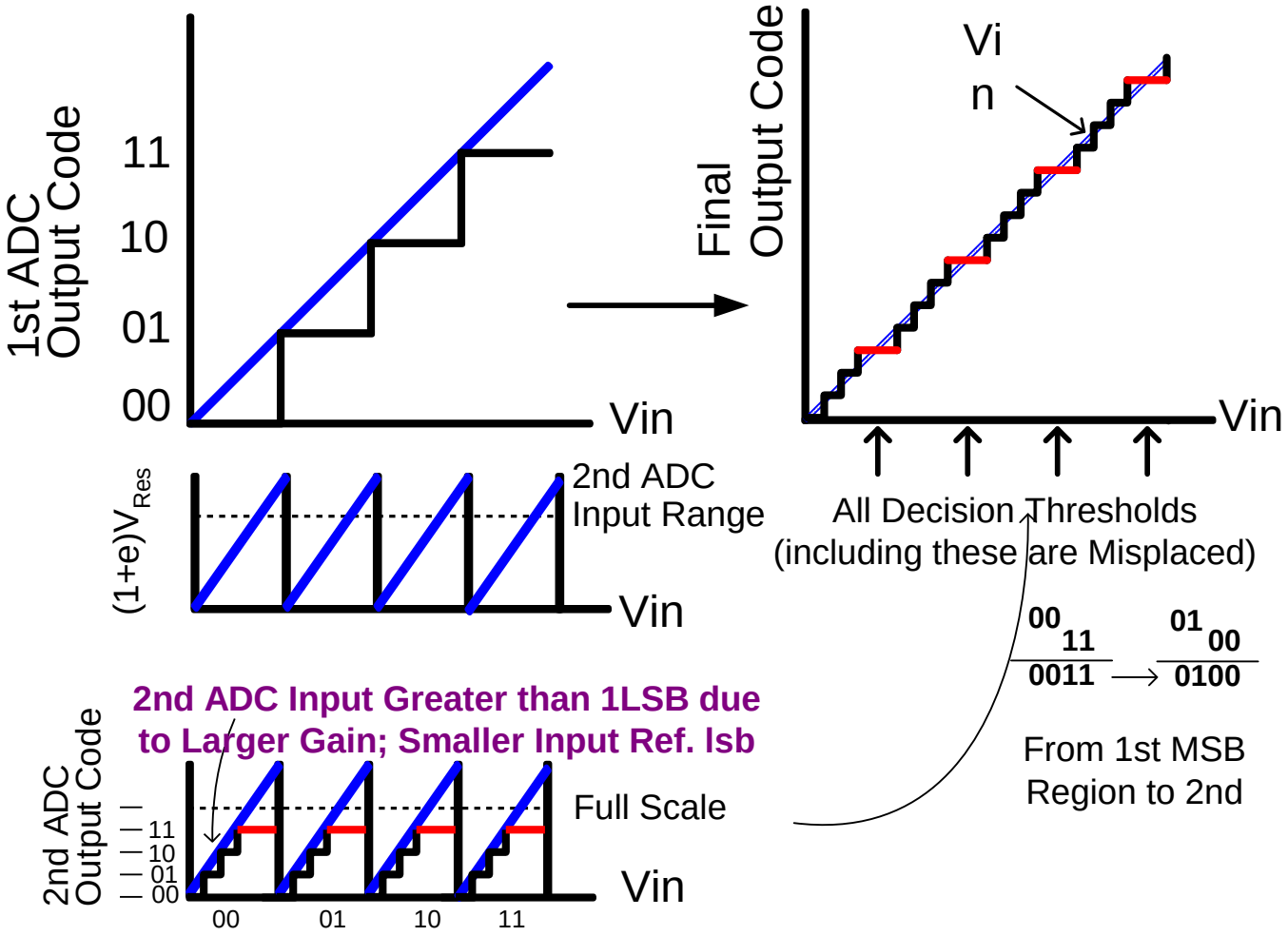
Two-Step ADC – DNL Error



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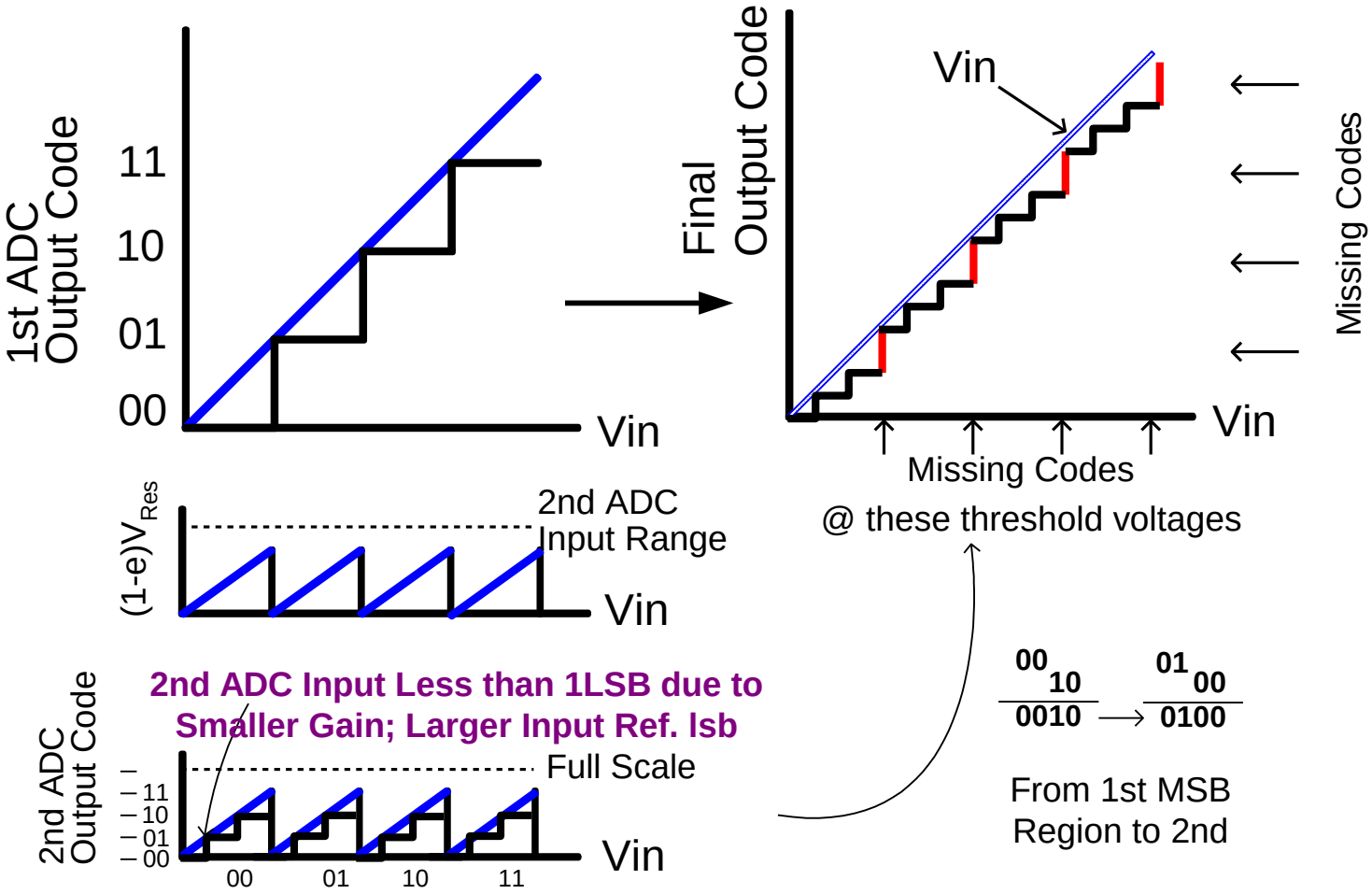
Two-Step ADC – Missing Codes



Real ADC with IDEAL DAC

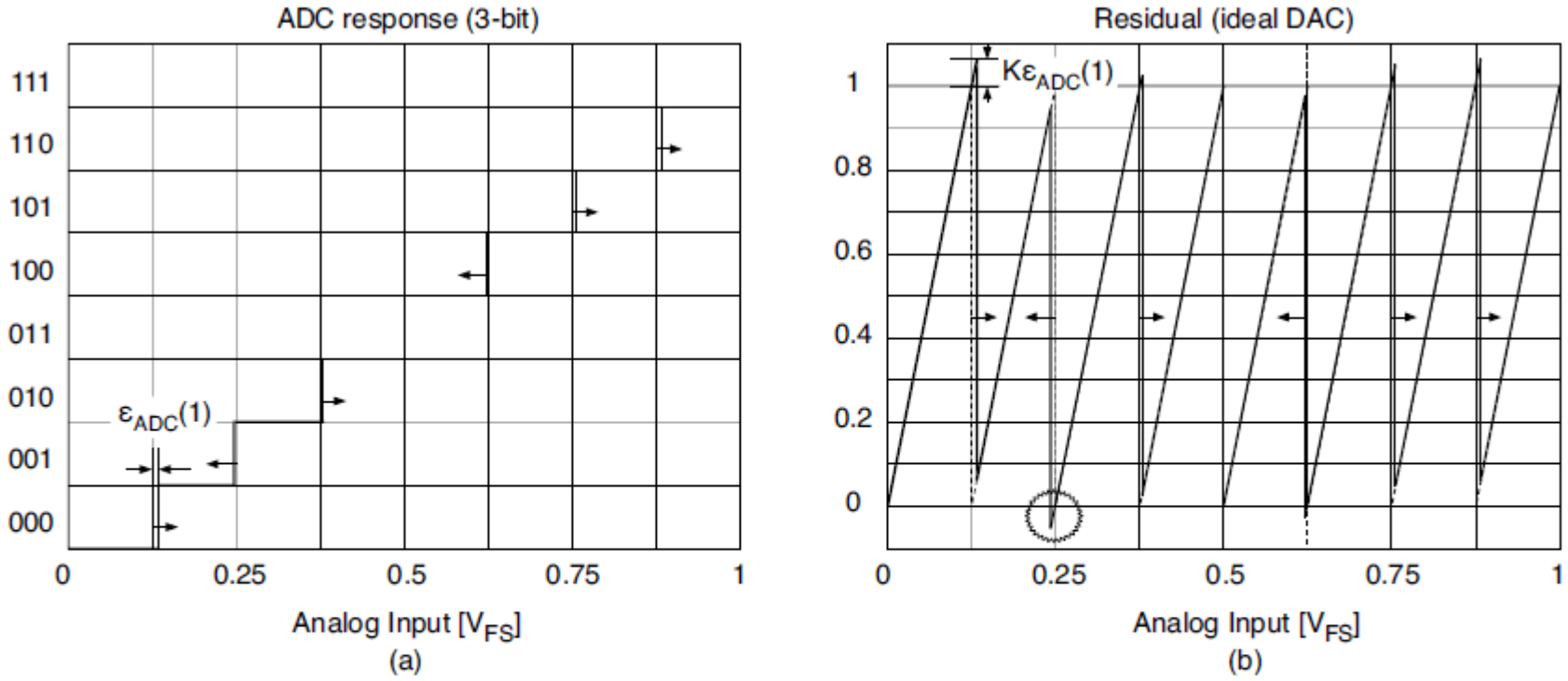


Figure 4.11. (a) Response of a real coarse ADC (3=bit). (b) Residue with ideal DAC.

[Ref: Maloberti's book]

IDEAL ADC with REAL DAC

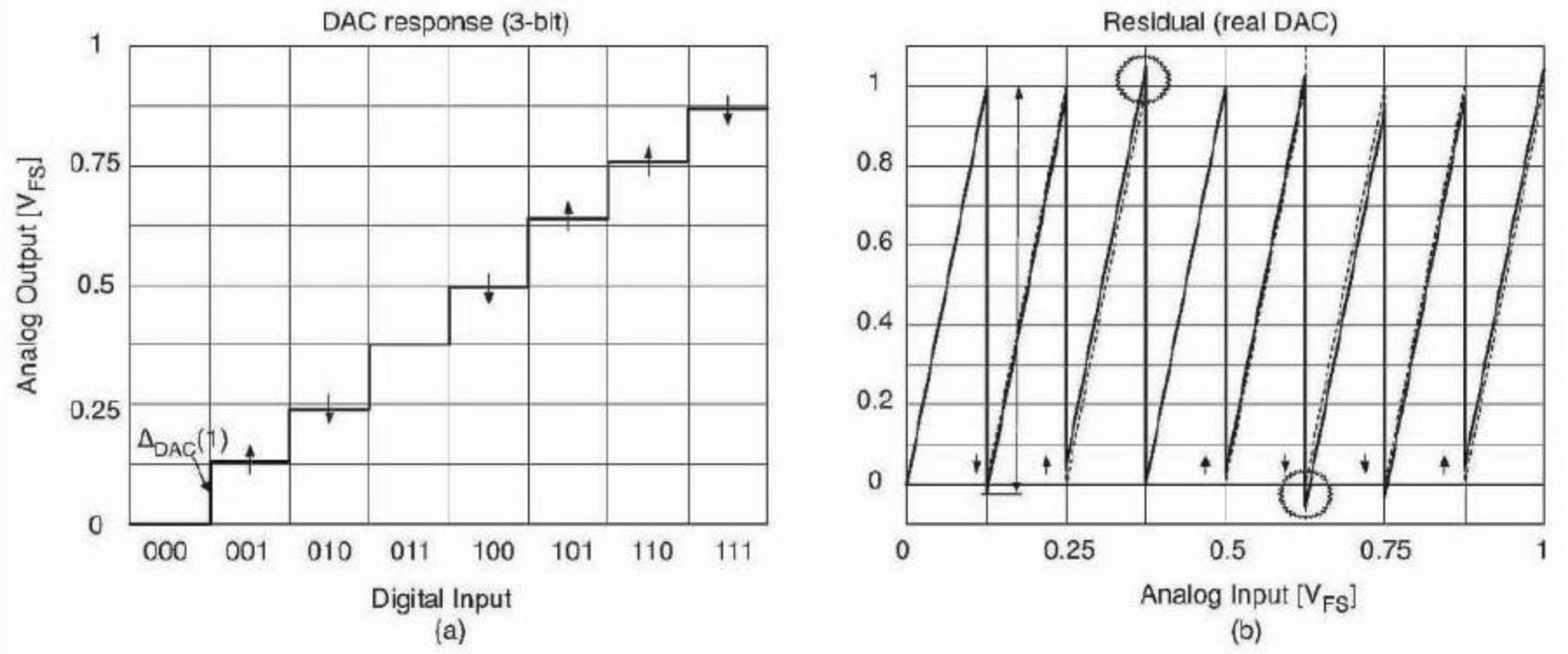
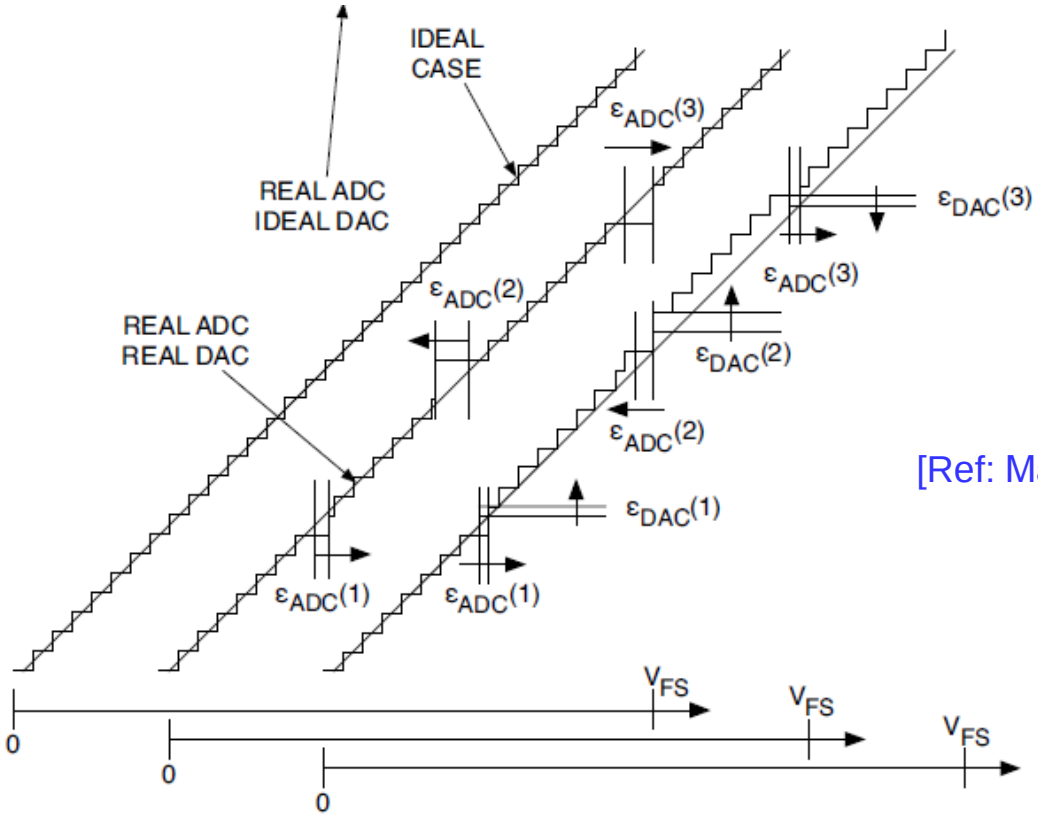


Figure 4.12. (a) Response of a real DAC (3=bit). (b) Residue with real DAC and ideal ADC.

[Ref: Maloberti's book]

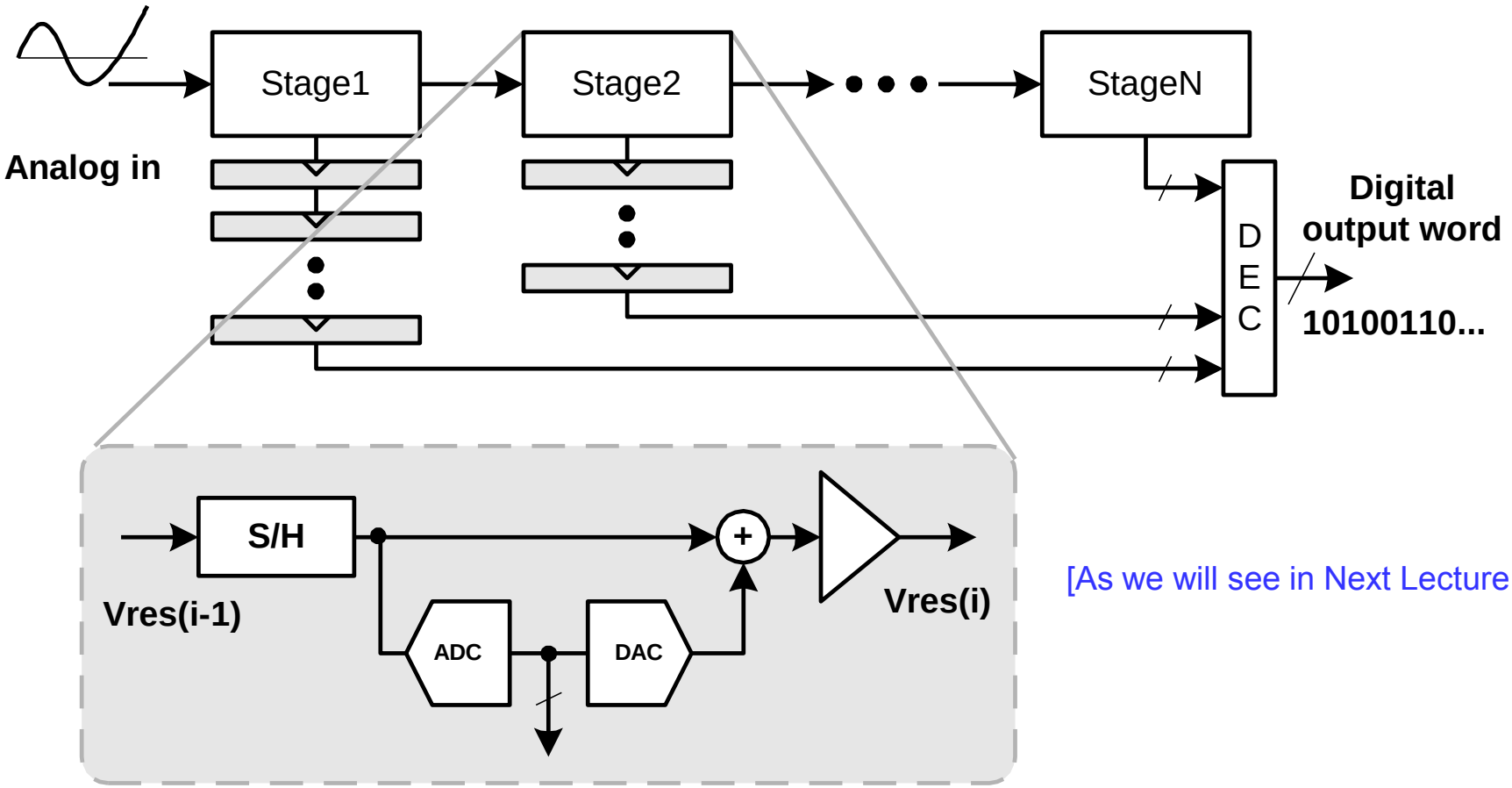


[Ref: Maloberti's book, pp. 162]

Figure 4.14. Static response of the two-step flash for ideal case and real *ADC* or *DAC*.

- Fig. 4.14 shows the input-output transfer curve for three different cases:
- ideal response (left curve), transfer characteristics with real *ADC* and ideal *DAC* (m iddle curve), and response with both *ADC* and *DAC* real (right curve).

Pipeline ADC (extension of 2-Step ADC)



[As we will see in Next Lecture,…..]

References

- Professor Boris Murmann Course slides 2012, Stanford University- EE315B course
- Professor Lotfi course slides, Ferdowsi University of Mahhad.