Analysis, design and implementation of zero-current transition interleaved boost converter

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Abstract: In this study, a new interleaved zero-current transition pulse-width modulation (PWM) boost converter, which uses only one auxiliary switch to provide soft-switching condition is presented and analysed. In order to reduce switching losses and to obtain high efficiency, a non-dissipative soft-switching cell is used. In the proposed interleaved converter, soft switching is obtained for all semiconductor devices. The main and auxiliary switches turn on and off under zero-current condition. Thus, the reverse-recovery losses of boost diodes are reduced and also, high efficiency is achieved owing to reduction of switching losses. Also, implementation of control circuit is simple since the proposed circuit is controlled by PWM method. Operating principles, theoretical analysis, the design procedure along with a design example are described and verified experimentally. Experimental results are presented to justify the validity of theoretical analysis.

1 Introduction

Current fed DC–DC converters are widely employed in industrial applications. Nowadays, more and more renewable energy sources are applied, but, most of these sources, such as fuel cells and solar cells provide low and unregulated output voltage [1–4]. Therefore for renewable power sources, high efficiency and high step-up DC–DC converters are necessary as an interface circuit. This interface circuit should absorb power from a low-voltage high-current source and provide a high DC voltage for load which is usually an inverter. Thus, the voltage should be boosted and regulated by using current fed converters as the interface circuit. When power rating increases, it is needed to connect converters in parallel to provide the output power. The interleaved structure is used in high-current and high-power applications because of its advantages such as power distribution and reduction of input current ripple as well as reduction of passive components and the electromagnetic interference (EMI) filter size [5–7]. When isolation is not necessary, boost converter is applied for the interface circuit because of its simple structure. Also, the boost converter is widely applied in single-phase power factor correction circuits [8], because of its continuous input current. In modern DC–DC converters, in order to reduce size and weight, switching frequency is increased [9]. However, high switching frequency will result in high switching losses and increased EMI. Therefore at high switching frequency, soft switching techniques such as zero-voltage transition (ZVT) and zero-current transition (ZCT) are applied to reduce switching losses and increase efficiency. These techniques provide soft switching condition while the control circuit remains PWM. Therefore switching losses and EMI are reduced. By operating under soft switching condition, DC–DC converters can be applied at higher switching frequency to further reduce the converter size and weight [10–18]. ZVT interleaved converters are proper techniques when MOSFET switches are used to reduce capacitive turn on losses as well as switching losses [19–21]. For higher power applications, where isolated-gate bipolar transistor switches are used owing to their lower conduction losses and cost, ZCT techniques are preferred to eliminate tailing current losses. Several interleaved ZCT PWM converters are introduced in [22–26]. In [22], two auxiliary switches are used to provide soft switching conditions. The current peak of semiconductor devices in the converter introduced in [23] is high although interleaved technique is used. In addition, di/dt is higher than the proposed interleaved boost converter, which results in higher EMI. In [24, 25], the main switches are turned on under the ZCT condition, but are turned off under the hard-switching condition. In this paper, a new interleaved ZCT PWM converter is introduced, which uses only one auxiliary switch. Furthermore, in this converter the current stresses of the main switches are low. Fig. 1 shows proposed interleaved ZCT boost converter. The main converter is composed of \( D_1, D_2, S_1 \) and \( S_2 \). The auxiliary circuit is composed of \( S_a, L_i, C_i, L_{S1}, L_{S2}, D_{p1} \) and \( D_{p2} \). The intrinsic anti-parallel diodes of main switches are \( D_{S1} \) and \( D_{S2} \). The output capacitance and load resistance are \( C_o \) and \( R_s \), respectively. The proposed converter operates like a conventional interleaved boost converter except during switching instances. \( L_i \) and \( C_i \) are resonant components, while \( S_a \) controls the resonant instant. \( L_{S1} \) and \( L_{S2} \) are snubber inductors of main switches. Auxiliary switch \( S_a \) is a unidirectional switch, whereas main switches are bidirectional switches. Complexity of a soft switching converter is determined by additional switches used because
each additional switch requires an additional gate drive signal which would increase the complexity of control circuit as well as the power stage. The proposed converter uses only one additional switch to provide soft switching condition for the main switches. Therefore this circuit has less complexity in comparison with the mentioned converters in the references. Also, it is important to notice that since the auxiliary circuit elements are not in the main power path, the current rating of auxiliary circuit elements is low.

2 Proposed ZCT PWM interleaved boost converters

In order to simplify the converter analysis, following assumptions are considered:

1. Output capacitor is large enough so that it can be replaced by a DC-voltage source.
2. Inductances \( L_1 \) and \( L_2 \) are equal (\( L_1 = L_2 \)).
3. All semiconductor devices are ideal.

To simplify the analysis, \( L_1 \), \( L_2 \) and \( C_o \) are replaced by current and voltage sources, respectively, as shown in Fig. 2.

It is important to notice that sources such as fuel cells, batteries and solar panels have low-output voltage level of about 48 V. Hence an efficient high step-up converter such as proposed interleaved boost converter is useful as the interface circuit. The converter operation consists of two symmetrical half cycles during each switching period. Therefore only half of a switching cycle is explained. In addition, it is assumed that converter operates at steady state.

Converter operation in half of the switching cycle can be divided into nine modes. The equivalent circuit for each operating mode and theoretical waveforms are illustrated in Figs. 3 and 4, respectively. The photograph of the original set-up is shown in the Fig. 5. Before the first mode it is assumed that main switch \( S_1 \) and auxiliary switch \( S_a \) are off and main switch \( S_2 \) is conducting \( L_2 \) current. Also, \( D_1 \) is conducting and \( C_r \) is charged to \( V_o \).

\[ t_1 - t_0 = \frac{L_{S1} I_m}{V_0} \]  

2.1 Mode 1: \([t_0 \rightarrow t_1]\) (Fig. 2a)

This mode begins by turning \( S_1 \) on. Owing to \( L_1 \), main switch \( S_1 \) is turned on under zero-current switching (ZCS) condition. Therefore the current flowing through \( S_1 \) increases linearly to \( L_1 \) current (\( I_m \)) and \( L_{S1} \) current decreases linearly from \( I_m \) to zero. At the end of this mode, \( S_1 \) current and \( L_{S1} \) current are \( I_m \) and zero, respectively. Duration of this mode is

At \( t_1 \), current of resonant inductance \( L_{S1} \) becomes zero. In this mode \( S_1 \) and \( S_2 \) are on and \( L_1 \) and \( L_2 \) are being charged.

2.2 Mode 2: \([t_1 \rightarrow t_2]\) (Fig. 2b)

At \( t_1 \), current of resonant inductance \( L_{S1} \) becomes zero. In this mode \( S_1 \) and \( S_2 \) are on and \( L_1 \) and \( L_2 \) are being charged.

![Proposed interleaved ZCS boost converter](image1)

**Fig. 1** Proposed interleaved ZCS boost converter

![Equivalent circuit of interleaved ZCS boost converter](image2)

**Fig. 2** Equivalent circuit of interleaved ZCS boost converter

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Fig. 3  Equivalent circuit of each operating mode

a  Mode 1  
b  Mode 2  
c  Mode 3  
d  Mode 4  
e  Mode 5  
f  Mode 6  
g  Mode 7  
h  Mode 8  
i  Mode 9  

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2.3 Mode 3: \([t_2 - t_3]\) (Fig. 2c)

This mode begins by turning \(S_a\) on to provide soft-switching for \(S_2\) turn off. By turning \(S_a\) on, a resonant starts between \(L_r\) and \(C_r\). Therefore auxiliary switch \(S_a\) turns on under ZCS condition. This mode ends when the \(C_r\) voltage reaches zero. Duration of this mode is

\[
t_3 - t_2 = \frac{T_r}{2}
\]

where \(T_r\) is the resonance period of \(L_r\) and \(C_r\). The voltage on \(C_r\) and the current through the auxiliary switch are obtained as

\[
V_{C_i}(t) = V_o \cos(\omega_1(t - t_2)) \quad (3)
\]

\[
I_{S_a}(t) = \frac{V_o}{Z_1} \sin(\omega_1(t - t_2)) \quad (4)
\]

where \(\omega_1 = 1/\sqrt{L_r C_r}\), \(Z_1 = \sqrt{L_r/C_r}\) and \(T_r = 2\pi\sqrt{L_r C_r}\).

In the equation, \(\omega_1\) and \(Z_1\) are the resonant frequency and resonant impedance, respectively.
2.4 Mode 4: \([t_3 - t_4]\) (Fig. 2d)

At \(t_2\), diodes \(D_{p1}\) and \(D_{p2}\) begin to conduct and \(C_r\) is discharged resonating with \(L_r\), \(L_{S1}\) and \(L_{S2}\). Therefore the currents through main and auxiliary switches are reduced. This mode ends when the current through main switches reaches zero.

\[
I_{S1}(t) = I_{S2}(t) = I_m - \frac{L_{eq} V_o}{L_{S1}} [1 - \cos(\omega_{eq}(t - t_3))] \tag{5}
\]

\[
I_{S3}(t) = \frac{V_o}{L_{eq}} - \frac{L_{eq} V_o}{L_{eq}} \frac{L_{eq}}{L_{S1}} [1 - \cos(\omega_{eq}(t - t_3))] \tag{6}
\]

\[
V_{C_i}(t) = -\frac{V_o}{\sqrt{1 + (2L_r/L_{S1})}} \sin(\omega_{eq}(t - t_3)) \tag{7}
\]

where \(\omega_{eq}\) and \(L_{eq}\) are the resonant frequency and equal inductance in this mode, respectively, and are obtained from the following equations

\[
\omega_{eq} = 1/\sqrt{L_{eq}C_r} \quad \text{and} \quad L_{eq} = L_r|L_{S1}|L_{S2}
\]

As the \(D_{p1}\) and \(D_{p2}\) are the conducting, the voltage on \(D_1\) and \(D_2\) increase as \(V_{C_i}\) decreases.

\[
V_{D1}(t) = V_{D2}(t) = V_o + \frac{V_o}{\sqrt{1 + (2L_r/L_{S1})}} \sin(\omega_{eq}(t - t_3)) \tag{8}
\]

2.5 Mode 5: \([t_4 - t_5]\) (Fig. 2e)

At \(t_4\), the currents through main switches \(S_1\) and \(S_2\) reach zero. Thus anti-parallel diodes \(D_{S1}\) and \(D_{S2}\) begin to conduct. This mode ends when the current through auxiliary switch \(S_a\) reaches zero at \(t_5\). \(V_{C_i}, I_{S1}, I_{S2}, V_{D1}, V_{D2}\) and \(I_{S3}\) can be calculated using (5)–(8).

2.6 Mode 6: \([t_5 - t_6]\) (Fig. 2f)

At \(t_5\), the current of auxiliary switch reaches zero. Thus, auxiliary switch \(S_a\) turns off under ZCS condition. Sum of \(D_{p1}\) and \(D_{p2}\) currents run through \(C_i\) and thus, the voltage across \(C_i\) increases. At the end of this mode anti-parallel diodes \(D_{S1}\) and \(D_{S2}\) turn off. During this mode \(S_2\) is turned off under ZCS condition.

2.7 Mode 7: \([t_6 - t_7]\) (Fig. 2g)

At \(t_6\), the anti-parallel diodes \(D_{S1}\) and \(D_{S2}\) turn off. In this mode, the current through \(L_{S2}\) and \(D_{p2}\) is constant and equal to \(I_m\). Also, the resonance between \(L_{S1}\) and \(C_r\) continues and the current through \(L_{S1}\) and \(D_{p1}\) decreases and thus, the current through main switch \(S_1\) increases. At the end of this mode the current through \(L_{S1}\) and \(D_{p1}\) reaches zero and the current of \(S_1\) increases to \(I_m\).

2.8 Mode 8: \([t_7 - t_8]\) (Fig. 2h)

In this mode, \(C_i\) is charged by the constant current \(I_m\) through \(L_{S2}\) and \(D_{p2}\). This mode ends when \(C_i\) voltage reaches \(V_o\).

\[
V_{C_i}(t) = V_{C_i}(t_f) + \frac{I_m}{C_i}(t - t_f) \tag{9}
\]

2.9 Mode 9: \([t_8 - t_9]\) (Fig. 2i)

At \(t_8\), the voltage on \(C_i\) is \(V_o\). Thus \(D_2\) turns on under zero voltage switching (ZVS) condition and \(D_{p2}\) turns off under ZVS condition. Since the voltage on \(C_r\) is clamped at \(V_o\), the voltage on \(D_{p2}\) and its current remain zero. In this mode the proposed converter behaves like a regular interleaved PWM boost converter.

3 Design procedure

This section presents design procedure for the proposed converter.

The converter specifications for 250 W converter are

- Output power \(P_o = 250\) W;
- Output voltage \(V_o = 200\) V;
- Input voltage \(V_{in} = 48\) V;
- Switching frequency of the main switches \(f_{sm} = 100\) kHz;
- Switching frequency of the auxiliary switch \(f_{S_a} = 200\) kHz.

The converter specifications for 50 W converter are

- Output power \(P_o = 50\) W;
- Output voltage \(V_o = 200\) V;
- Input voltage \(V_{in} = 48\) V;
- Switching frequency of the main switches \(f_{sm} = 100\) kHz;
- Switching frequency of the auxiliary switch \(f_{S_a} = 200\) kHz.

The design procedure of this converter is explained in four steps as following.

3.1 Resonant elements \((C_r, L_r, L_{S1} \text{ and } L_{S2})\)

In order to obtain soft switching condition for both main switches, the maximum current through each snubber inductor should be greater than \(I_m\) in the fifth mode. In this condition, the current through the main switches will be negative and the main switches body diodes will conduct. Considering 20% over design, the following relation is obtained

\[
I_{S_a} = \frac{V_o}{L_{S1}} = 1.2I_m \tag{10}
\]

where

\[
I_m = \frac{P_o}{2V_{in}} \tag{11}
\]

\[
I_{S_a} = \frac{P_o}{2V_{in}} \Rightarrow I_{S_a} = \frac{V_o}{2Z_r} = 2.4I_m \Rightarrow Z_r = \frac{V_o}{2.4I_m} \tag{12}
\]

where \(P_o\) is the output power. Also, the resonant period should be negligible in comparison with the switching
Thus, the resonant frequency is selected at least ten times greater than the switching frequency.

\[ T_{\text{res}} = 2\pi\sqrt{\frac{L_r}{C_r}} \geq \frac{T_{\text{sw}}}{10} \quad (13) \]

where \( T_{\text{res}} \) and \( T_{\text{sw}} \) are the resonance and switching periods, respectively.

By using (12) and (13), \( T_{\text{res}}, L_r \) and \( C_r \) can be obtained. Before turning the main switches off, the auxiliary circuit should operate to reduce the current through the main switches to zero. Therefore converter minimum duty cycle is
\[ D_{\text{min}} = \frac{t_5 - t_3}{T_{\text{sw}}} = \frac{\pi - \sin^{-1}((2Z_r/V_o)f_m)}{\alpha T_{\text{sw}}} \]  

(14)

where \( L_{S1} \) and \( L_{S2} \) are the snubber inductors of main switches and their value can be calculated like any snubber inductor. By calculating \( L_s \) value and using (10)–(13), \( T_{\text{res}}, L_c \) and \( C_r \) can be obtained.

### 3.2 Selection of \( S_1, S_2 \) and \( S_a \)

The peak current and voltage stresses of switches are obtained from the following equations

\[ V_{S1,2} = V_{Sa} = V_{o\max} \]  

(15)
\[ I_{sw1,2} = \frac{P_o}{2V_{in}} + \frac{\Delta I_L}{2} \]  
(16)

\[ I_{Sa} = \frac{V_o}{2} \]  
(17)

where \( \Delta I_L \) is the current ripple of each input inductor.

### 3.3 Selection of \( D_1, D_2 \) and \( D_o \)

The current peak and voltage stresses of the diodes are obtained from the following equations

\[ V_{D1,2\ max} = 2V_{o\ max} \]  
(18)

\[ I_{D1,2\ max} = \frac{P_o}{2V_{in}} + \frac{\Delta I_L}{2} \]  
(20)

\[ I_{D1,2\ max} = \frac{P_o}{2V_{in}} + \Delta I_L \]  
(21)

### 3.4 Selection of \( L_1, L_2 \) and \( C_o \)

The value of inductances \( L_1 \) and \( L_2 \) and capacitance value of \( C_o \) can be obtained exactly like a conventional PWM converter [27].

### 4 Experimental results

The schematic of the prototype converter is shown in Fig. 6 and the experimental results of the proposed converter topology are shown in Fig. 7. Also the photograph of the original set-up is shown in Fig. 5 that shows the main and control circuit prototypes. The proposed ZCT interleaved boost converter is implemented for input voltage of \( V_{in} = 48 \) V DC and output voltage of \( V_o = 200 \) V DC operating at \( f_{sw} = 100 \) kHz. In the implemented prototype, IRGBC20U is used as main and auxiliary switches. MUR860 diodes are used as \( D_1 \) and \( D_2 \) and MUR460 diodes are used as \( D_{p1} \) and \( D_{p2} \). A 10 nF and a 100 \( \mu \)F capacitors are used as \( C_r \) and \( C_o \), respectively. Inductors values for \( L_1 \) and \( L_2 \) are 300 \( \mu \)H, and \( L_r \) is 8 \( \mu \)H. Inductors values for \( L_{S1} \) and \( L_{S2} \) are 16 \( \mu \)H. Figs. 7 and 8 show the current and voltage waveform of the main and auxiliary switches, respectively, for 250 W converter. The resonant capacitor voltage is presented in Fig. 9. Also, Figs. 10 and 11 show the current and voltage waveform of the main and auxiliary switches, respectively, for 50 W converter. It can be observed that the main switch is turned on under ZCS condition for both converters. Also for both converters, the main switch current is reduced to zero just before turning this switch off. In addition, ZCS is achieved for the auxiliary switch at turn on and turn off instants. Fig. 12 shows the efficiency against output power for the proposed interleaved boost converter and its hard-switching counterpart. The losses of each semiconductor device in the proposed converter and hard-switching converter are compared in Table 1. Table 1 shows detail comparison between the simulation results of the proposed converter and the traditional hard-switched counterpart.

![Fig. 13 Schematic of control circuit of the proposed interleaved boost converter](image)

TI494 IC is applied for PWM controller. Also, 74123 IC is used as monostable. The delay circuit is implemented using RC circuits. Also, ICL7667 is applied as gate drive.
switching converter is similar to the proposed converter and is obtained by eliminating the auxiliary circuit. For practical implementation, RCD snubber circuit is applied for the hard-switching converter. According to Table 1, as expected, owing to reduced reverse-recovery losses of the boost diodes and switching losses, the proposed converter has higher efficiency than the conventional PWM hard-switching converter.

The schematic of the control circuit for the proposed converter is shown in Fig. 13.

5 Conclusion

In this paper, a new interleaved ZCT PWM boost converter is introduced. This converter uses only one auxiliary switch to provide soft-switching condition for the main and auxiliary switches. The main and auxiliary switches turn on and off under zero-current switching condition. This converter has higher efficiency than the conventional PWM hard-switching converter because of the reduced reverse-recovery losses of boost diodes and switching losses. Also, the proposed converter is controlled by PWM method. According to the experimental results, the efficiency is improved by about 2.9%. This converter is analysed and the design procedure is presented. The presented experimental results verify the theoretical analysis.

6 References