Design and improvement of a soft switching high step-up boost converter with voltage multiplier

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Abstract: A new soft switching high step-up boost converter is proposed in this study. Coupled inductors technique is used along with voltage multiplier in order to provide high-voltage gain and reduce voltage stress across semiconducting elements. Using an active clamp circuit, soft switching condition is provided for both the main and auxiliary switch which reduces the switching losses and improves the circuit efficiency as well as power density. The reverse recovery problem of diodes is alleviated due to the existence of the leakage inductances of the coupled inductors in series with diodes. The circuit performance is investigated and theoretical analysis is provided. A 200 W 40 V input to 400 V output laboratory prototype of the proposed converter is implemented, and the experimental results show the proper performance of the proposed converter.

1 Introduction

Efficient utilisation of diverse renewable sources of energy is one of the biggest challenges in the field of power and energy. Using power electronic interfacing circuits is necessary for connecting renewable sources of energy to the grid. Solar cell systems are the most desirable sources of renewable energy due to the availability of the sun light and flexibility in panel installation. In order to improve the efficiency of photovoltaic (PV) panels and preventing problems such as shadow effect on panels and mismatch between panels, using modular PV systems are preferred [1, 2]. In such systems, in order to extend the input voltage of PV cells and connecting them to a high-voltage bus, a DC–DC high step-up converter with high efficiency is used [3]. In addition, these converters are being used in many applications from emergency power systems, fuel cell and power supplies to high-intensity discharge lamps [4, 5].

In isolated converters, high-voltage gain can be achieved by proper adjustment of the transformers’ turn ratio. However, the efficiency is usually low. Non-isolated converters are commonly used in low-to-medium power range applications due to their higher efficiency, high power density and low price [6]. Achieving high-voltage gain is not possible in the basic boost converter because of low efficiency, high conduction loss and severe reverse recovery of the output diode. Coupled inductor-based converters are of the favourable structures between the presented high step-up converters. In these structures, high-voltage gain can simply be obtained by adjusting the turn ratio of the coupled inductors. Also, the voltage spikes across the main switches of the converter caused by the leakage inductance can be suppressed by incorporating a lossless passive clamp circuit [7] or active clamp solution [8, 9]. The main drawback of these converters is the high voltage across the output diode which necessitates a snubber circuit or high-voltage diodes [10].

A three-level boost converter is presented in [11]. Compared with the basic boost converter, the three-level boost converter can halve the voltage stress across the semiconducting elements, which is suitable for high-output voltage applications. Switching losses and electromagnetic interferences will reduce due to low-voltage stress. However, hard switching performance of the semiconducting components and the reverse recovery problem of the output diode are of the most serious problems of this converter. In [12], a boost converter integrated with a fly-back converter is presented for obtaining high step-up voltage gain. In this structure, the boost converter acts as a passive clamp circuit and recycles the leakage inductance energy.

In [13], a single switch high step-up converter based on the coupled inductors is introduced. In this converter, the energy stored in the leakage inductance of the coupled inductors is recycled by passive clamp circuit which reduces the voltage spike across switch and diodes. As a result, switches with small on-resistance can be employed which contributes to efficiency improvement. However, this converter has a complex structure. A coupled inductor-based interleaved boost converter is introduced in [14]. High step-up voltage gain is resulted by using voltage multiplier and coupled inductors. The input current ripple is reduced because of using cross-coupled inductors as well as the interleaved structure. Thanks to using winding cross-coupled inductors and interleaved structure, the input current ripple is reduced in this converter. Also, the leakage inductance energy is recycled and soft switching condition is provided for switches using active clamp circuit. High-voltage stress of the output diodes is of the shortcomings of this converter which make the use of high-voltage diodes indispensable. A boost converter based on coupled inductors is presented in [15]. The clamp capacitor is placed at the charging path of the output capacitor which not only absorbs the leakage energy, but also increases the voltage gain.

2 The proposed soft switching high step-up boost converter

Based on the discussions mentioned in the Introduction, it can be understood that in a solar system, a switching converter is needed which, in addition to high efficiency, has low-voltage stress across its switches so that high-quality low-priced MOSFETs could be utilised. To achieve these purposes, the proposed high gain converter is introduced in this section. At first, the proposed converter is presented and its operating principles are explained. Then, the converter characteristics and the design procedure are investigated, after which simulation and experimental results are shown. Finally, a thorough conclusion of the mentioned discussions is provided. Fig. 1 shows the proposed converter schematic. This converter is made of using three techniques: voltage multiplier circuit, coupled inductors and active clamp for creating soft switching condition. Due to high-voltage gain, the
The operating mode is shown in Figs. 4 and 5. The inductance of the coupled inductors can provide soft switching assumptions are made to explain the operating modes of the switches is in an interleaving manner. The converter is controlled by two pulsed with duty cycles larger than 0.5° and 180° phase shift.

In order to explain the operating modes of the proposed converter, the coupled inductors are modelled which can be seen in Fig. 2. Each switching cycle consists of five operating modes. The key waveforms of the proposed converter are illustrated in Fig. 3, and the equivalent circuit of the proposed converter in each operating mode is shown in Figs. 4 and 5. The following assumptions are made to explain the operating modes of the proposed converter:

1. The capacitors are considered ideal. Also, \( C_{o1} = C_{o2} = C_{o3} = C_{o4} \).
2. The coupled inductors are considered as shown in Fig. 2, and their other associated parasitic elements are omitted.
3. All switches and diodes are ideal and the voltage drop across them is neglected.

Mode 1 \((t_0, t_1)\): In this mode, switch \( S_1 \) and diodes \( D_2 \) and \( D_4 \) are conducting. Switch \( S_2 \) is turned off, and diode \( D_1 \) is off due to reverse voltage \( V_{C_{o1}} + nV_{in} \) across it. Magnetising inductance \( L_m \) and leakage inductance \( L_k \) are charged by the input voltage source. During this mode, \( D_3 \) is not conducting because of reverse voltage \( V_{C_{o2}} + V_{C_{o3}} \) across it. The output capacitors \( C_{o2} \) and \( C_{o4} \) are charged by the secondary windings of the coupled inductors, and \( C_{o3} \) and \( C_{o4} \) provide the load required energy. This mode ends when \( S_1 \) is turned off. The equivalent circuit during this mode is shown in Fig. 4. The important equations in this mode are as follows:

\[
I_{t_0}(t) = I_{t_0}(t_0) + \frac{V_{C_{o1}}}{nL_m}(t - t_0)
\]

\[
I_{t_0}(t) = I_{t_0}(t_0) + \frac{nV_{in} - V_{C_{o2}}}{nL_k}(t - t_0)
\]

Mode 2 \((t_1, t_2)\): At \( t = t_1 \) switch \( S_1 \) turns off, and the anti-parallel diode \( D_{32} \) starts to conduct because of resonance between \( L_k \) and parallel capacitor of \( S_2 \), so \( S_2 \) can be turned on under the zero voltage switching (ZVS) condition. Also, the voltage across \( S_1 \) becomes limited to \( V_{C_{o1}} \). \( D_2 \) is still conducting, but \( D_1 \) is in off state because of the reverse voltage \( V_{C_{o2}} + V_{C_{o2}} - V_{C_{o1}} \). Also, voltage \( (V_{C_{o2}})(n) \) is applied across the magnetising inductance and makes its current to be increased. Also, since \( D_1 \) is not conducting, the voltage across the leakage inductance is reversed and the large voltage \( V_{C_{o2}} + V_{C_{o2}} - V_{C_{o1}} \) is applied across it which makes \( n_{12} \) and \( n_{13} \) windings current to promptly reduce. Moreover, \( D_3 \) is still off due to the reverse voltage \( V_{C_{o2}} + V_{C_{o2}} \). At the end of this mode, the leakage inductance current \( I_{Lk} \) equals with the magnetising inductance current \( I_{Lm} \), which in turn makes the currents flowing through \( n_{12} \) and \( n_{13} \) windings to become zero, and \( D_2 \) along with \( D_4 \) turn off at zero current. In this mode, the leakage inductance current equation is as follows:

\[
I_{t_1}(t) = I_{t_1}(t_1) - \frac{V_{C_{o1}} + (V_{C_{o2}}) - V_{in}}{nL_k}(t - t_1)
\]

Mode 3 \((t_2, t_3)\): \( D_3 \) turns on at the start of this mode, and the reverse voltage \( V_{C_{o2}} + V_{C_{o2}} - V_{C_{o1}} \) is applied across \( D_2 \) and the reverse voltage \( V_{C_{o2}} + V_{C_{o2}} \) is applied across \( D_4 \). Also, due to the shift in \( n_{12} \) winding voltage polarity, \( D_1 \) starts to conduct. In this mode, the magnetising inductance voltage is reversed and both magnetising and leakage inductance currents reduce. The output capacitors \( C_{o1} \) and \( C_{o3} \) are charged via the secondary windings of the coupled inductors, and the load is supplied by the output capacitors \( C_{o2} \) and \( C_{o4} \). The leakage inductance current reaches to \( I_{Lm} \), the anti-parallel diode \( D_{36} \) turns off at zero current. The important equations in this mode are as follows:

\[
I_{t_2}(t) = I_{t_2}(t_2) - \frac{V_{C_{o2}}}{nL_m}(t - t_2)
\]

\[
I_{t_3}(t) = I_{t_3}(t_3) - \frac{nV_{C_{o2}} - nV_{in} - V_{C_{o2}}}{nL_k}(t - t_3)
\]
and reverse voltage $V_{C_{o1}} + V_{C_{o2}} - V_C$ across $D_2$, these diodes are still reverse biased. The negative voltage $-(V_{C_{o1}}/n)$ is applied across the magnetising inductance during this mode, as a result, $L_m$ is being discharged. Also, the negative voltage across the leakage inductance $L_{lk}$ is $-V_{C_{o1}} + (1 + (1/n))V_{C_{o1}} + V_{in}$, so $L_{lk}$ current is also being decreased. The leakage inductance current becomes zero at the end of this mode and increases at the negative direction. In this mode, the leakage inductance current equation is as follows:

$$I_{l_{lk}}(t) = I_{l_{lk}}(t_1) - \frac{nV_{C_{o1}} - (1 + n)V_{C_{o1}} - nV_{in}(t - t_1)}{nL_{lk}}$$  \hspace{1cm} (6)

Mode 5 ($t_4$, $t_5$): $S_2$ is turned off at the start of this mode, and the leakage inductance total current makes $D_5$ to conduct. In this situation, $S_1$ can be turned on in a ZVS manner. The reverse voltage $V_{C_{o1}} - V_{C_{o5}}$ is applied across the output diode $D_1$ and make it off. Also, the large voltage $V_{in} + (V_{C_{o4}}/n)$ is applied across the primary leakage inductance and its current increases with a sharp slope and the output diode $D_5$ current is reduced fast. Also, due to the reverse voltages $V_{C_{o3}} + V_{C_{o3}}$ and $V_{C_{o2}} + V_{C_{o2}} - V_C$ which are applied across $D_4$ and $D_2$, respectively, these diodes are still reverse biased. The output capacitor $C_{o3}$ is charged by the secondary winding of the coupled inductors, $n_{13}$, and the output capacitors $C_{o1}$, $C_{o2}$ and $C_{o4}$ provide the required load energy. As the leakage inductance current $I_{l_{lk}}$ reaches to the magnetising inductance current $I_{l_{m}}$, the output diode $D_2$ turns off under the zero current switching (ZCS) condition and this mode ends. The leakage inductance current equation in this mode is as follows:

$$I_{l_{lk}}(t) = I_{l_{lk}}(t_1) + \frac{nV_{in} + V_{C_{o1}}}{nL_{lk}}(t - t_1)$$  \hspace{1cm} (7)

3 Steady-state analysis

In this section, specifications of the proposed converter are stated, and its advantages and disadvantages are investigated.

3.1 Voltage gain of the proposed converter

When $S_1$ is turned on (mode 1), the output capacitor $C_{o4}$ is charged by $n_{13}$ winding. Also, the output capacitor $C_{o2}$ is charged by $n_{12}$ winding and capacitor $C_c$. So, $C_{o2}$ and $C_{o4}$ voltages can be expressed as follows:

$$V_{C_{o2}} \cong nV_{in}$$  \hspace{1cm} (8)

$$V_{C_{o4}} \cong nV_{in} + V_C$$  \hspace{1cm} (9)

where $n$ is the turn ratio of the coupled inductors which is defined as follows:

$$n = \frac{n_{13}}{n_{11}} = \frac{n_{12}}{n_{11}}$$  \hspace{1cm} (10)

Applying voltage-second balance to magnetising inductance $L_m$ would result in voltage equations of $C_{o1}$ and $C_c$ as follows:

$$V_{C_{o1}} = \frac{1 + nD}{1 - D} \cdot V_{in}$$  \hspace{1cm} (11)

$$V_C = \frac{V_{in}}{1 - D}$$  \hspace{1cm} (12)

During the third and fourth modes, the output diode $D_4$ is conducting and $C_{o3}$ is charged by $n_{13}$ winding. So, by writing Kirchhoff’s Voltage Law (KVL) in the output loop and using above equations, the capacitor $C_{o3}$ voltage equation is calculated as follows:

$$V_{C_{o3}} = \frac{V_{in}}{1 - D}$$  \hspace{1cm} (13)

The output voltage of the proposed converter is the summation of $C_{o1}$, $C_{o2}$, $C_{o3}$ and $C_{o4}$ voltages. So, the output voltage and the voltage gain of the proposed converter can be obtained as follows:

$$V_o = \frac{2(1 + n)}{1 - D} \cdot V_{in}$$  \hspace{1cm} (14)

$$G_v = \frac{V_o}{V_{in}} = \frac{2(1 + n)}{1 - D}$$  \hspace{1cm} (15)

In Fig. 6, the voltage gain of the proposed converter against different duty cycles is shown. The turn ratio of the coupled inductors is considered to be 2. As can be seen, the proposed converter can provide large voltage gain with moderate duty cycles, so extreme duty cycles can be prevented.

3.2 Voltage stress of stress across switches and diodes

Regarding equations obtained for capacitor voltages, the voltage stress across switches and diodes is achieved as follows. The voltage stress across switch $S$ and diode $D_1$

$$V_S = V_{D_1} = V_C = \frac{V_{in}}{1 - D}$$  \hspace{1cm} (16)

The voltage stress across $D_2$ and $D_3$

$$V_{D_2} = V_{D_3} = \frac{n + 1}{1 - D} \cdot V_{in}$$  \hspace{1cm} (17)

The voltage stress across $D_4$ and $D_5$

$$V_{D_4} = V_{D_5} = V_{C_{o3}} + V_{C_{o4}} = \frac{n}{1 - D} \cdot V_{in}$$  \hspace{1cm} (18)
In Fig. 7, the voltage stress variations of the main switch against different duty cycles are plotted. As can be observed, the voltage stress across the main switch is low even.

![Fig. 4](image_url) The equivalent circuit of the proposed converter in each operating mode
(a) Mode 1, (b) Mode 2, (c) Mode 3

![Fig. 5](image_url) The equivalent circuit of the proposed converter in each operating mode
(a) Mode 4, (b) Mode 5

3.3 Condition of ZVS realisation

In order to realise the ZVS condition, the leakage inductance should satisfy the following condition (it is assumed $C_s = C_{s1} = C_{s2}$):

\[
L_{m} < \frac{V_{in}}{f_{sw} \cdot n_{sc} \cdot C_{s}}
\]
where $\Delta t$ is defined as follows:

$$\Delta t = \frac{V_i \cdot L_m \cdot D \cdot T}{(L_m + L_b)}$$

To design the snubber capacitor, the following equation can be used which is the basic equation for designing the snubber capacitor in power electric circuits:

$$C_s > \frac{i_{sw} \cdot t_f}{2 \cdot k \cdot V_{sw}}$$

where $t_f$ is the voltage across the switch in off time, $V_{sw}$ is the switch current before turn-off instant, $i_{sw}$ is the guarantee coefficient for creating soft switching condition, which is considered about 0.2. $k$ is the switch current deterioration time. $C_{s1}$ and $C_{s2}$ are designed based on (21).

### 3.4 Performance comparison

The properties of the proposed converter are compared with the basic boost converter and some recent high step-up converters. The results are shown in Table 1. As can be seen, the proposed converter has the highest voltage gain among all the compared converters, so high duty ratios can be prevented. The voltage stress across the main switch of the proposed converter is the least between other converters; as a result, high-quality low-voltage switches can be employed. Also, the voltage across the output diode is lower than those of [1–3], so the reverse recovery problem has been improved in the proposed converter. There is an additional switch in the proposed converter compared with the basic boost converter and the converter presented in [1], but soft switching condition is created for the main switch which improves circuit efficiency and power density of the proposed converter. It can be concluded that compared with the presented converters in [6, 8–10], the proposed converter is a better option to be used in the renewable energy-based high-voltage gain application.

### 4 Experimental results of the proposed converter

In order to prove the discussions mentioned in the previous section, the proposed converter is implemented as a laboratory prototype. The input voltage is 40 V and the output voltage is 400 V for 200 W output power. The switching frequency is selected as 50 kHz. Other specifications of the implemented converter are reported in Table 2. The experimental results are depicted in Figs. 8 and 9. The voltage and current waveforms of the main switch are shown in Fig. 8a. As can be seen, the voltage spikes across switch caused by the leakage inductance of the coupled inductors are well absorbed and the voltage stress across switch is clamped at almost a quarter of the output voltage. Also, as it is shown, at turn-on instance, the switch current is negative which shows the current flow through the switch anti-parallel diode and proves the ZVS operation of the switch. As it is shown in Fig. 8b, one can see that the auxiliary switch performs under the ZVS condition because the negative switch current shows that the switch anti-parallel diode is conducting. Also, the voltage stress across the auxiliary switch is a quarter of the output voltage. As a result, low-voltage switches with small on-state resistance could be selected for both the main and auxiliary switch. The voltage and current waveforms of diodes $D_1$ and $D_2$ are shown in Figs. 8c and d, respectively. The soft turn-on of $D_1$ can be observed, and ZCS turn-off of $D_2$ is clear which alleviates its associated reverse recovery problem. Also, the voltage stress across $D_2$ is half of the output voltage. The voltage and current waveforms of diodes $D_3$ and $D_4$ are shown in Figs. 9a) and 9b), respectively. The voltage stress across these diodes is a quarter of the output voltage which helps improve their associated reverse recovery problem. It can be seen that due to the existence of the leakage inductance of the coupled inductors in series with diodes, currents flowing through diodes decrease softly, and the reverse recovery problem of these diodes is alleviated.

### Table 1 Performance comparison of the proposed converter with the basic boost converter and converters presented in [6, 8–10]

<table>
<thead>
<tr>
<th>Voltage Gain</th>
<th>Stress Voltage on Switches</th>
<th>Stress Voltage on Output Diode</th>
<th>Number of Switches</th>
<th>Number of Diodes</th>
<th>Soft Switching</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional boost converter presented in [6]</td>
<td>$1-DV_{in}$</td>
<td>$V_o$</td>
<td>2</td>
<td>1</td>
<td>no</td>
</tr>
<tr>
<td>Converter presented in [8]</td>
<td>$2+n-nD$</td>
<td>$V_o$</td>
<td>1</td>
<td>4</td>
<td>yes</td>
</tr>
<tr>
<td>Converter presented in [9]</td>
<td>$1+2n-nD$</td>
<td>$V_o$</td>
<td>1</td>
<td>3</td>
<td>yes</td>
</tr>
<tr>
<td>Converter presented in [10]</td>
<td>$1+2n-nD$</td>
<td>$V_o$</td>
<td>1</td>
<td>2</td>
<td>yes</td>
</tr>
<tr>
<td>The proposed converter</td>
<td>$1+2n-nD$</td>
<td>$V_o$</td>
<td>1</td>
<td>2</td>
<td>yes</td>
</tr>
<tr>
<td>n</td>
<td>$1+2n-nD$</td>
<td>$V_o$</td>
<td>1</td>
<td>4</td>
<td>yes</td>
</tr>
</tbody>
</table>

![Fig. 6](image6.png) The voltage gain variations of the proposed converter against different duty cycles

![Fig. 7](image7.png) The voltage stress across the main switch against different duty cycles

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The proposed converter dynamic response of the proposed converter is tested under a step load change condition (full load to no-load transient condition) and its result is provided in Fig. 10. The efficiency of the proposed converter for different output powers is plotted in Fig. 11. The maximum efficiency achieved is 97% at 80% of the nominal load. As the output power increases, the conduction losses of elements increase and the efficiency drops.

5 Conclusion

In this paper, a soft switching high step-up boost converter is presented and its operating principles are explained. Then the properties of the proposed converter are investigated and the main equations are extracted. To verify the exactness of theoretical analysis, a laboratory prototype of the proposed converter is
performs under the ZVS condition, too. Reverse recovery problem condition is provided for the main switch, and the auxiliary switch. The experimental results prove the proper performance of the proposed converter. So, the proposed converter has high efficiency and good performance and is suitable to be used in applications based on renewable sources of energy.

References


Fig. 11 The efficiency of the proposed converter for different output powers

Table 2 Specifications of the laboratory prototype of the proposed converter

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
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</thead>
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<tr>
<td>P</td>
<td>output power</td>
<td>200 W</td>
</tr>
<tr>
<td>V_in</td>
<td>input voltage</td>
<td>40 V</td>
</tr>
<tr>
<td>V_o</td>
<td>output voltage</td>
<td>400 V</td>
</tr>
<tr>
<td>f_S1</td>
<td>main switch switching frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td>f_S2</td>
<td>auxiliary switch switching frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td>L_m</td>
<td>magnetising inductance</td>
<td>100 μH</td>
</tr>
<tr>
<td>L_k</td>
<td>leakage inductance</td>
<td>5 μH</td>
</tr>
<tr>
<td>N</td>
<td>turn ratio of the coupled inductors</td>
<td>1</td>
</tr>
<tr>
<td>S1, S2</td>
<td>MOSFET switches</td>
<td>IRFP260</td>
</tr>
<tr>
<td>D1-D4</td>
<td>diode</td>
<td>MUR460</td>
</tr>
<tr>
<td>C_C</td>
<td>capacitor</td>
<td>2 μF</td>
</tr>
<tr>
<td>C_o1–C_o4</td>
<td>output capacitors</td>
<td>47 μF</td>
</tr>
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