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# Soft-Switching Non-Isolated High Step-Up DC-DC Converter With Continuous Input Current for PV Application

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## ABSTRACT

In this paper, a high step-up DC-DC boost converter is introduced, which utilises the coupled inductor and switched capacitor techniques to increase voltage gain, adjustable by changing the turn ratio of the coupled inductors. Additionally, the leakage inductance of the coupled inductors reduces the reverse recovery problem of the output diode. The boost inductor in the input stage ensures continuous input current, thereby extending the lifetime of the input battery or improving the performance of renewable power sources. The proposed converter employs an active clamp technique to achieve soft switching for both the main and auxiliary switches over a wide range of output power, ensuring zero-voltage switching during both on and off states. Key features of the proposed converter include continuous input current, soft switching, high voltage gain, and a simple structure. A 200 W laboratory prototype is implemented, and the results are provided.

## 1 | Introduction

Over the past several years, high step-up DC-DC converters have had a remarkable role in environment-friendly energy systems that comprise solar photovoltaic (PV) systems, wind energy and fuel cells (FCs), as can be seen in Figure 1. Recently, high step-up DC-DC converters have garnered attention due to the fact that the output voltage of these resources typically falls below 24–48 V, insufficient to meet the demand of DC/AC grids, which typically require voltages lower than 600 V, as cited in references [1, 2]. Generally, DC-DC high step-up converters are classified into two categories, including isolated and non-isolated converters. Isolated high step-up converters which utilise transformers with high turns ratio are used widely; however, non-isolated converters are preferred in situations where isolation is not mandatory since they provide a reduction in size, weight, and volume [3]. The first and also the most basic step-up non-isolated converter is the conventional boost converter. Although the ideal boost converter can increase the input voltage up to infinity theoretically, it cannot be achieved in practice due to efficiency reduction. Moreover, since the voltage stress of the semiconductor devices is equal to the output voltage, it is not an appropriate choice for high step-up applications [4, 5]. It is also possible to use basic converters in a cascade structure to increase the output voltage; however, their efficiency suffers from processing the power twice. Additionally, voltage stress of the switch in the second stage is still high, and there may exist some stability problems [6, 7].

To increase the voltage gain, other techniques are proposed in [8–10] in which coupled inductors, voltage multiplier cells and switched capacitor techniques are the most important ones. Achieving maximum voltage gain, the time duration through which the output diode is on is short; hence, all the converter topologies discussed above suffer from the diode reverse-recovery problem. In some recent literature [11, 12], the reverse-recovery problem of the output diode is alleviated by using the coupled


**FIGURE 1** | Diagram of a grid connected renewable energy system.

inductors. The leakage inductance of the coupled inductor also reduces the reverse recovery problem of the output diodes; therefore, it reduces the relative reverse-recovery losses and EMI (Electromagnetic Interference) noise as well [13]. In [14], to increase voltage gain, a high step boost converter is presented utilising switched capacitor and coupled inductor techniques. However, this converter suffers from high conduction losses and a complexing topology, resulting in a high cost. The magnitude of the input current ripple is another remarkable point to take into account in high step-up boost converters. Also, discontinuous input current can adversely impact the performance of the maximum power point tracking (MPPT) system in photovoltaic (PV) applications. Therefore, in recent years, converters with continuous input current and low ripple are preferred, as highlighted in references [6, 15].

To achieve high efficiency, soft switching techniques are proposed in [16–26]. In [16–18], boost converters are introduced in which a snubber passive circuit to achieve soft switching conditions is used. Furthermore, input current in these structures is continuous, resulting in reducing the input capacitor. However, voltage gain in these topologies is similar to a classical boost converter. In [19], another high step-up boost is introduced, which, by utilising ZVT (Zero Voltage Transition) technique, soft switching performance is obtained in the whole range of output power in comparison to converters that use the active clamp technique. In reference [20], a ZVT high step-up boost converter is introduced. This converter takes advantage of high voltage gain, a low number of components and high efficiency. In the negative side, this converter suffers from discontinuous input current. In reference [21], an interleaved boost converter is presented, which, via the ZVT technique, obtains soft switching performance in a wide range of output power. However, this converter suffers from a high number of switches. In addition, voltage gain is relatively high, and stress voltage across the main switch is relatively low, resulting in using switches with low RDS(On). Since a diode is used in the input of the converter, the conduction loss of the input diode is high, and this converter suffers from high conduction losses, resulting low efficiency. In [23], a converter based on the active clamp technique to obtain a soft switching manner is presented. In this topology, to increase the voltage gain, coupled inductor and switched capacitor techniques are used. In addition, by using a three-level structure, this converter takes advantage of low-stress voltage across the main switches, leading to low conduction loss. However, the soft switching condition is lost in light loads, which result in decreased efficiency in light loads.

In converters in [24–26], new high step-up DC-DC converters are proposed. In these converters, by utilising the active clamp technique, soft switching performance is achieved. In addition, since ultra-high voltage gain is achieved in these converters, stress voltage across the main switch is low, resulting in high efficiency. However, not only is the input current in this converter discontinuous, but also the soft-switching range is lost in the light loads. In [27–29] high step-up DC-DC converters are introduced in which soft switching manner and high voltage gain are achieved. On the negative side, complexity is the main drawback of these converters. To achieve ultra-high voltage gain, as shown in [30–32], these converters employ coupled inductors and switched capacitor techniques, which reduce the conduction losses of the switches. Also, converters in [30, 31] take advantage of continuous input current and low components, which is another advantage of these converters. However, both of these converters suffer from hard switching performance. Although converters in [32] provide a soft switching manner, complexity is the main disadvantage of this topology.

In this paper, a soft-switched high step-up converter with continuous input current is presented. To enhance the limited voltage gain of the typical boost converter and maintain the benefits of its continuous input current ripple, coupled inductors are integrated into the boost converter alongside the output stage. By employing this technique, not only is the voltage gain increased, but the voltage stress across the power switch is also alleviated. Also, since all diodes are turned off in ZCS (Zero Current Switch) condition, the reverse recovery problem of them is reduced in the proposed converter. In addition, as the input inductor of the boost converter is retained, the input current ripple remains low, leading to improved performance for renewable power sources. This issue eliminates the necessity for a bulky input filter capacitor to compensate for the large current ripple. Soft switching performance is another remarkable feature of the proposed converter, which provides a soft switching range in the whole range of output power, resulting in high efficiency. So, the advantages of the proposed converter can be highlighted as below:

- Achieving high voltage gain without requiring a large duty cycle

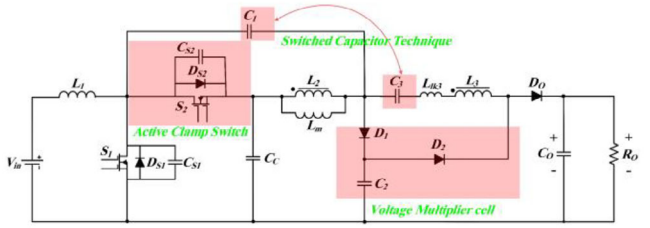



**FIGURE 2** | Schematic of the proposed soft-switched high step-up converter.

- Obtaining soft-switching performance across a wide range of output power
- Ensuring continuous input current
- Reducing voltage stress across the switches
- Mitigating the reverse recovery losses of the output diodes, thereby improving efficiency
- High power density and low cost

The rest of this paper is organised as follows. In Section 2, the proposed circuit is introduced, and its structure and operating principles are explained. The steady-state analysis and design guidelines are covered in Section 3. In Section 3.7, the experimental result is discussed, and a loss distribution analysis along with efficiency is provided in Section 4. Finally, conclusions are discussed in Section 5.

## 2 | Operating Principles of the Proposed Converter

The schematic of the proposed soft-switched high step-up converter can be seen in Figure 2. The proposed converter is essentially a boost converter with the incorporation of a pair of coupled inductors in series with the output stage, aiming to extend the voltage gain. By adding two diodes and switched capacitor cells, the leakage energy of the coupled inductors is absorbed to clamp the voltage across the main switch. Also, by replacing the input diode with an active clamp switch loss, is significantly decreased. As can be seen in the characteristic of the proposed converter, $S_1$ is the main switch and $S_2$ is the auxiliary switch. Also, the input inductor is defined by $L_1$, and the coupled inductors are modelled by a magnetising inductance $L_m$, and the equivalent leakage inductance is $L_{lk}$. In this schematic, $C_C$ is the clamp capacitor, and $C_1$, $C_2$, and $C_3$ are switched capacitors. $D_1$ and $D_2$ are utilised to provide voltage second balance for secondary coupled inductors. Do and Co are the output diode and output capacitor of the converter, respectively. At steady state, there are seven operating modes within one switching period. The key waveforms of the proposed converter are illustrated in Figure 3. Finally, to simplify the analysis, we suppose that all components are ideal, and the operating modes of the introduced converter are shown in Figure 4. In the proposed converter, capacitors are large in a way that their voltage ripple is fixed within a switching period.

***Mode 1 [$t_0$-$t_1$]*** **(**Figure 4a**):** In this mode, the main switch is on and the auxiliary switch is off. Diodes $D_1$ and $D_O$ are reverse biased. $L_1$ is charged by the input voltage source, and the magnetising inductance $L_m$ is also charged by the $V_{CC}$-$V_{C1}$ voltage. In this mode, $C_2$ capacitor is discharged by diode $D_2$. The output load is fed through the output capacitor *Co*. The following equations are established through this mode.

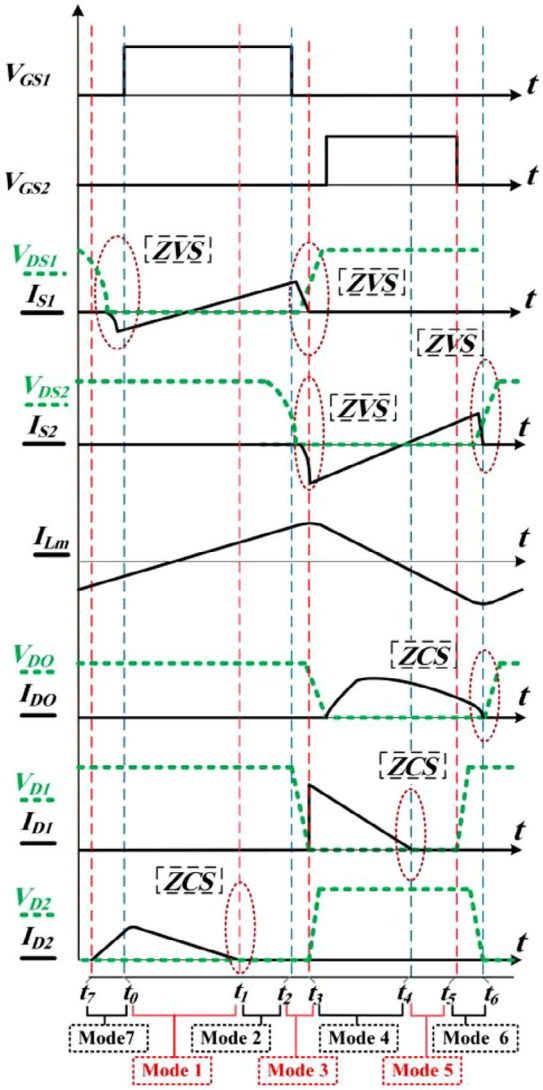



**FIGURE 3** | The key waveforms of the proposed converter.

$$I_{L1} = I_{L1}\ (t_0) + \frac{V_{in}}{L_{in}}(t - t_0) \tag{1}$$

$$I_{Lm} = I_{Lm}\ (t_0) + \frac{V_{CC} - V_{C1}}{L_m + L_{Lk}}(t - t_0) \tag{2}$$

$$i_{Llk}\ (t) = \frac{2V_{C1} + V_{C3} - V_{C2} - V_{CC}}{L_{lk}}\ (t - t_0) \tag{3}$$

***Mode 2 [$t_1$-$t_2$]*** **(**Figure 4b**):** At $t_1$, $C_2$ the capacitor is completely discharged and $D_2$ is reversed so that the current of $L_1$ and $L_2$ is achieved to zero. At the end of this mode, the main switch is turned off.

***Mode 3 [$t_2$-$t_3$]*** **(**Figure 4c**):** At the commencement of this mode, the snubber capacitor of $S_1$ starts to charge linearly to achieve active clamp voltage. The summation of $L_1$ and $L_m$ currents pass

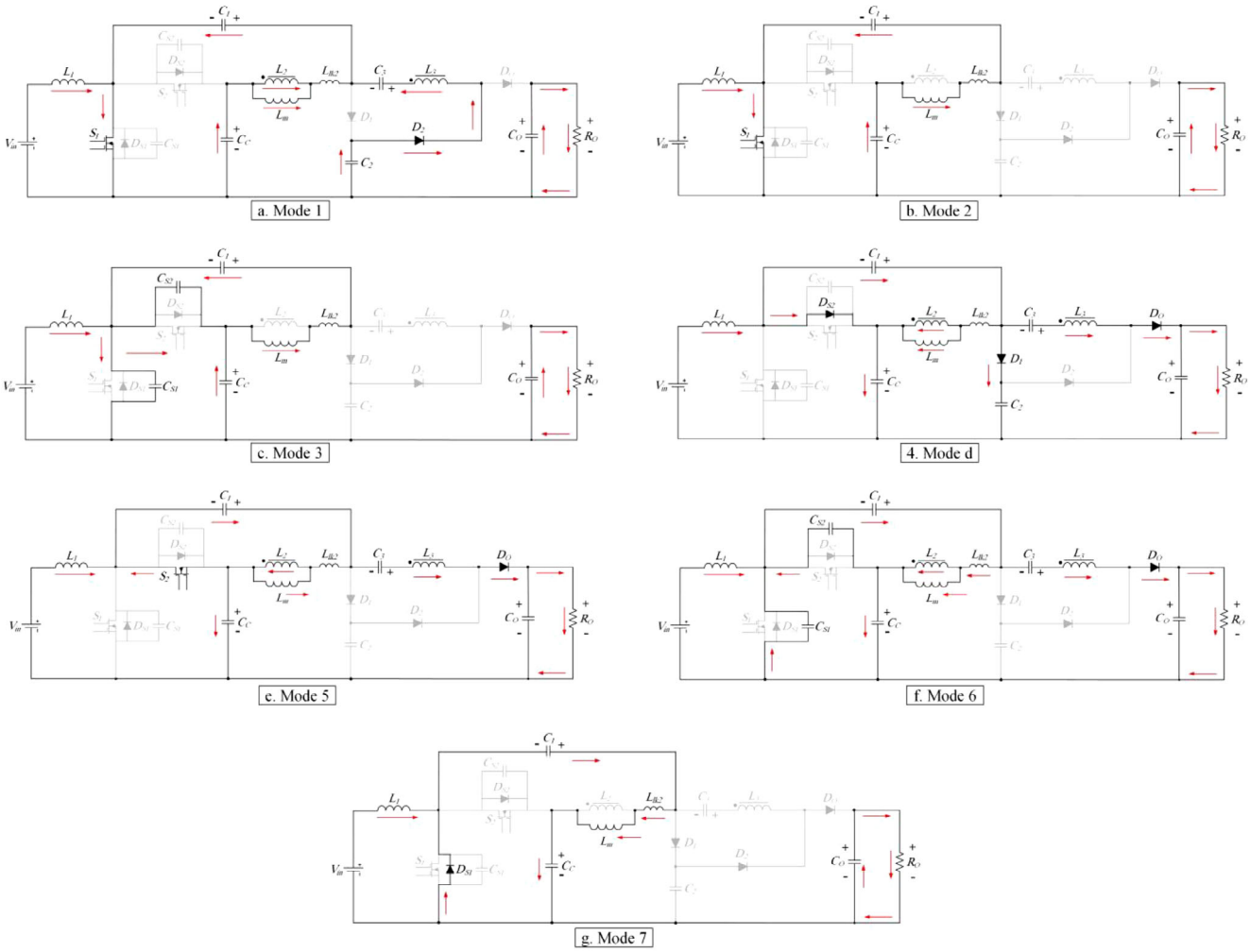



**FIGURE 4** | Equivalent circuits of converter operating modes.

through the $C_{S1}$. Also, in this mode, a resonant start between $L_{lk1}$ and $C_{SA,}$ which during this resonant $C_{SA}$ is being completely discharged, by reaching $C_{S1}$ to voltage clamp capacitor, this mode ends. The equations of this mode are as below:

$$V_{CS1}\ (t) = \frac{I_{Lin} + I_{Llk2}}{C_{S1}}\ (t - t_1) \tag{4}$$

$$\Delta t_3 = t_3\ -\ t_2 = \frac{V_{CC}}{I_{Lin} + I_{Llk2}}\ C_{S1} \tag{5}$$

***Mode 4 [$t_3$-$t_4$]*** **(**Figure 4d**):** At the beginning of this mode, $V_{SA}$ becomes zero, and the anti-parallel diode of the auxiliary switch conducts. By conducting this diode, Capacitor $C_C$ is charged by the input voltage source and Lin. The magnetising inductance transfers energy to the output via the secondary winding Ns. Also, $D_O$ starts to conduct in ZCS manner due to $L_{lk}$. In addition, $C_2$ capacitor is charged by conducting $D_1$. This mode ends when the $D_1$ current reaches zero. The below equations are obtained for this mode.

$$i_{Llk}\ (t) = i_{Llk}\ (t_3) - \frac{\frac{V_{C2}+V_{C3}-V_O}{n}}{L_{lk2}}\ (t - t_3) \tag{6}$$

$$I_{Lm} = I_{Lm}\ (t_3) - \frac{\frac{V_{C2}+V_{C3}-V_O}{n}}{L_m}\ (t - t_3) \tag{7}$$

***Mode 5 [$t_4$-$t_5$]*** **(**Figure 4e**):** At the beginning of this mode, the auxiliary switch is switched on and the summation of Lin and $S_1$ currents is entered into the $C_1$ capacitor. Also, in this mode $L_m$ current direction is changed. This mode ends when the auxiliary switch is turned off.

$$i_{DO-peak} = \frac{P}{(1-D)\,V_O} \tag{8}$$

$$I_{Lm} = I_{Lm}\ (t_4) - \frac{\frac{V_{CC}+V_{C1}+V_{C3}-V_O}{n}}{L_m}\ (t - t_4) \tag{9}$$

***Mode 6 [$t_5$-$t_6$]*** **(**Figure 4f**):** At this mode, the auxiliary switch is turned off and a resonant start occurs between $C_{S1}$, $C_{S2}$ and $L_{lk2}$ in a way that $C_{S1}$ is discharged and $C_{S2}$ is completely charged. This mode ends when $C_{S1}$ discharges.

$$V_{CS1}\ (t) = V_{CC}\ - \frac{I_{Llk2}\,(t_5)}{C_{S1} \parallel C_{S2}}\ (t - t_5) \tag{10}$$

$$\Delta t_6 = t_6\ -\ t_5 = \frac{(C_{S1} \parallel C_{S2})\,V_{CC}}{I_{Llk2}\,(t_5)} \tag{11}$$

***Mode 7 [$t_6$-$t_7$]*** **(**Figure 4g**):** At the commencement of this mode, the anti-parallel diode of the main switch conducts. Also in this mode, $L_{lk2}$ current reaches to $L_m$ current output diode that is turned off. In addition, since the anti-parallel diode of the

main switch conducts, the main switch can turn on under ZVS performance. In the next sections, voltage gain, voltage stress of the proposed converter and design of the inductors as well as capacitors are investigated.

## 3 | Analysis of the Proposed Converter

In this section, the introduced converter is evaluated under steady-state conditions, and it includes the formulation of equations for both voltage gain and voltage stress across components. Additionally, the design process for passive elements is presented.

### 3.1 | Conversion Ratio

When the main switch is on in mode 1, the voltage Vin is linearly applied across Lin. Conversely, when the main switch is turned off in mode 4, Vin-$V_{CC}$ is applied across Lin. By employing a voltage-second balance to Lin, the voltage across $C_C$ can be determined.

$$V_{CC} = \frac{V_{in}}{(1-D)} \tag{12}$$

In the first mode, the magnetising and leakage inductances are connected in series. The coupling coefficient, display as K, is defined as follows:

$$K = \frac{L_m}{L_m + L_{lk}} \tag{13}$$

Thus, the voltage across $L_m$, when the main switch is on is equal to:

$$V_{lm} = K(V_{CC} - V_{C1}) \tag{14}$$

And also, during the mode 4, when the switch is Off, the voltage across $L_m$ is equal to:

$$V_{lm} = -KV_{C1} \tag{15}$$

By writing voltage second balance for $L_m$, $V_{C1}$ is obtained as following:

$$V_{C1} = \frac{DV_{in}}{(1-D)} \tag{16}$$

Furthermore, in the fourth mode, during which the power switch is in the off state, the voltage across the magnetising inductance is equal to:

$$V_{lm} = K(V_{CC} - V_{C2}) \tag{17}$$

As both Equations (15) and (17) are derived from the fourth mode, they can be set equal to each other to determine $V_{C2}$, as illustrated below:

$$V_{C2} = (1+D)\frac{V_{in}}{(1-D)} \tag{18}$$

On the other hand, by writing the KVL rule from the first mode, $VL_m$ is achieved as below:

$$V_{lm} = (V_{C1} + V_{C3} - V_{C2})K \tag{19}$$

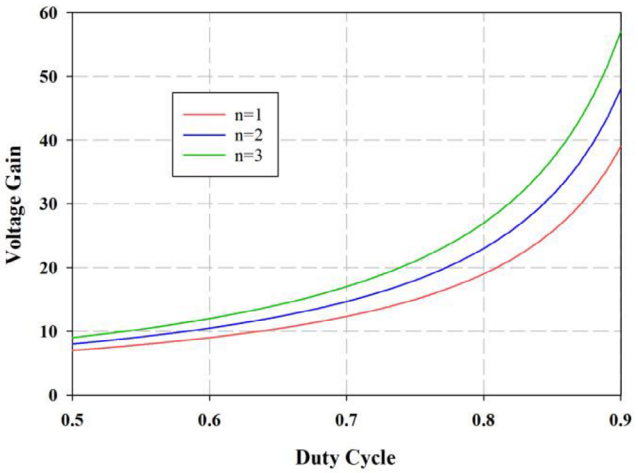



**FIGURE 5** | Voltage Gain Ratio vs. duty cycle for different turn ratios (n).

By substituting $V_{C1}$ and $V_{C2}$ from Equation (16) as well as Equation (18), and also since Equations (14) and (19) are both derived from the first mode, so, they can be equalised to obtain $V_{C3}$, as follows:

$$V_{C3} = (2-D)\frac{V_{in}}{(1-D)} \tag{20}$$

By writing KVL in fourth mode, we have:

$$-V_{CC} + \frac{1}{K}V_{lm} + nV_{lm} - V_{C3} + V_O = 0 \tag{21}$$

So, by replacing $V_{CC}$ and $V_{C3}$ from (12) and (20), $VL_m$ is achieved as follows:

$$V_{lm} = \frac{(3-D)\frac{V_{in}}{(1-D)} - V_O}{\frac{1}{K} + n} \tag{22}$$

As Equations (15) and (22) are achieved both from mode4, we can set them equal to obtain $V_{C1}$ as follows:

$$V_{C1} = \frac{V_O(1-D) - (3-D)V_{in}}{(1+nK)(1-D)} \tag{23}$$

Finally, by substituting $V_{C1}$ from Equations (16) in (23), voltage gain is achieved as below:

$$\frac{V_O}{V_{in}} = \frac{D(1+nK) + (3-D)}{(1-D)} \tag{24}$$

Figure 5 shows Voltage Gain Ratio vs. duty cycle for different turn ratios (n). As it can be seen, by increasing the turn ratio, higher voltage gains are achieved. Also, Figure 6 illustrates a comparison of voltage gains between the proposed converter and converters featured in [18, 20, 23, 25]. Evidently, the proposed converter exhibits a higher voltage gain compared to the converters referenced in [18, 20, 23]. Additionally, it demonstrates desirable features such as soft switching performance, low voltage stress, and continuous input current. While the proposed converter may have a lower voltage gain than the converter in [25], it compensates by requiring fewer components in comparison to its counterpart.

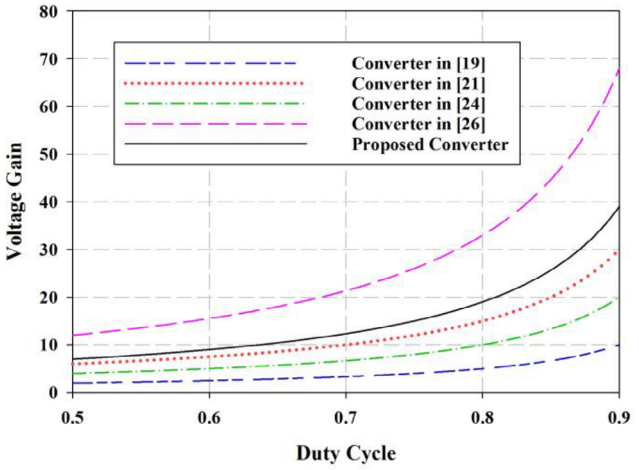



**FIGURE 6** | Comparison of voltage gain: proposed converter vs. other converters in [18, 20, 23, 25] (n = 1 and coupling factor (k) = 1).

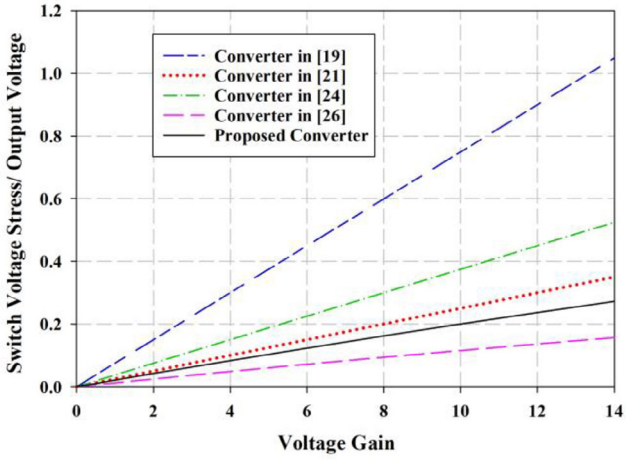



**FIGURE 7** | Voltage stress of the switch versus the voltage gain of the proposed converter compared with other converters in [18, 20, 23, 25] (n = 1 and k = 1).

**TABLE 1** | Current and voltage stress of semiconductor elements.

| Components | Current stress | Voltage stress |
|---|---|---|
| Switch $S_{1,2}$ | $\frac{P_o}{V_{in}} + \frac{V_{in}}{L_1}DT + \left(\frac{D^2(2D-n)T}{(1-D)^2}\right)\frac{V_{in}}{L_{lk}}$ | $\frac{V_{in}}{1-D}$ |
| Diode $D_1$ | $\frac{P_o}{V_{in}} + \frac{V_{in}}{L_1}DT$ | $\frac{V_{in}}{1-D}$ |
| Diode $D_2$ | $\frac{(n+2)V_{in} - V_o(1-D)}{L_{k1}}T_{sw}$ | $\frac{V_{in}(1+\mathrm{D})}{1-D}$ |
| Diode $D_o$ | $\frac{I_o}{1-D}$ | $\frac{V_{in}(1+\mathrm{D})}{1-D}$ |

### 3.2 | Voltage Stress of the Semiconductor Elements

The voltage and current stress values corresponding to various semiconductor components are reported in Table 1. Due to the incorporation of a passive clamp circuit, the voltage stress on the main switches, when this switch is in the off state (mode 4), equals $V_{CC}$, as utilised in Equation (12). This voltage stress is sufficiently low, enabling the use of high-quality MOSFETs with lower on-resistance. This, in turn, helps to minimise conduction losses in the circuit. Also, from mode 4, by writing the KVL rule, the stress voltage of $V_{D2}$ is achieved as follows:

$$V_{D2} = \frac{2V_{in}}{(1-D)} \tag{25}$$

Similarly, by applying the KVL rule in mode 1 and substituting $V_{C1}$ as well as $V_{C2}$ from Equations (16) and (18), it enables the calculation of the voltage stress on $D_1$ and $D_O$ as below:

$$\begin{aligned} -V_{C1} - V_{D1} + V_{C2} &= 0 \\ V_{D1} &= \frac{V_{in}}{(1-D)} \end{aligned} \tag{26}$$

$$\begin{aligned} -V_{C2} - V_{DO} + V_O &= 0 \\ V_{DO} = V_O &- (1+D)\frac{V_{in}}{(1-D)} \end{aligned} \tag{27}$$

For the axillary switch $S_2$, we have:

$$V_{S2} = V_{CC} \tag{28}$$

Figure 7 illustrates the relationship between the voltage gain and the voltage stress on the main switches. It also provides a comparison with converters from [18, 20, 23, 25]. Notably, even at higher voltage conversion ratios, the voltage stress on the power switch in the proposed converter is lower than that of the compared converters except converter [25]. This allows for the utilisation of cost-effective, low-voltage MOSFETs with reduced on-resistance, contributing to minimised conduction losses and overall circuit cost.

### 3.3 | Design of Magnetic Inductance

The calculation of the magnetising inductance can be performed using the following procedure:

$$V_{Lm} = Lm\frac{\Delta I_{Lm}}{\Delta t} \tag{29}$$

In which $V_{Lm}$ according mode 1 is calculated as follows:

$$V_{lm} = V_{CC} - V_{C1} \tag{30}$$

So, magnetising inductance is calculated as below:

$$Lm = \frac{DV_{in}}{\Delta I_{Lm}.f_{sw}} \tag{31}$$

The Tables 2 and 3 show specification of all elements and inductors respectively.

### 3.4 | Design of Capacitors

For designing the capacitors, when the switch is in the on state, $C_C$ is discharged by the magnetising inductance current, and simultaneously, $C_1$ is charged by this current. Consequently, the

**TABLE 2** | Important parameters of the implemented prototype.

| Parameter/ Component | Value | Component | Value |
|---|---|---|---|
| Input voltage ($V_{in}$) | 30V | $L_{m1} = L_{m2}$ | 10μH |
| Output voltage ($V_O$) | 400V | $L_{lk1}$ | 3μH |
| Output power ($P_O$) | 200W | $L_1$ | 300μH |
| Frequency ($f_{sw}$) | 100 kHz | $S_1, S_2$ | NTP011N15MC |
| Experimental Efficiency | %96.5 | $D_1$ | BYV32-200 |
| $C_C, C_1, C_2, C_3$ | 4.7 μF/160V | $D_2, D_O$ | MUR460 |
| $C_{S1}$ | 4.7 nF/150V | n | 1 |
| $C_{S2}$ | 2.2 nF/150V | $C_O$ | 22μF/400V |

**TABLE 3** | Winding parameters of the coupled inductors.

| | Proposed Converter | | |
|---|---|---|---|
| **Parameter** | $L_1$ | $L_2$ | $L_3$ |
| Number of wires turns | 71 | 11 | 11 |
| Wire length [cm] | 520 | 55 | 55 |
| Wire cross section [mm] | 1.5 | 1 | 1 |
| DC resistance [Ω] | 12mΩ | 3mΩ | 3mΩ |
| Core | EI 33-29 | EI 25 | |

voltage ripples across these capacitors are identical. The design of the capacitors is determined based on the desired voltage ripple, as outlined below:

$$C_1 = \frac{I_{Lin}(1-D)}{f\Delta V_{C1}} \tag{32}$$

$$C_C = \frac{I_{Llk2}D}{f.\Delta V_{CC}} \tag{33}$$

$$C_2 = C_3 = \frac{(1-D)I_{Lm}}{f(n+1)*\Delta V_o} \tag{34}$$

$$C_{s1}, C_{s2} > \frac{i_{sw}*t_f}{2Y_v V_{sw}} \tag{35}$$

In which, Vsw represents the maximum voltage across the switch, $i_{Sw}$ is the switch current, $Y_v$ is a coefficient which is usually selected around 0.25 and $t_f$ denote the fall time.

## 3.5 | Soft Switching Criteria

To achieve the desired soft-switching conditions, precise design of the auxiliary circuit and resonant components is essential. A careful trade-off is necessary when selecting values for $n_3$ and $n_2$, as these can impact both the converter's voltage gain and the voltage stress on semiconductors. Furthermore, the soft-switching operation is sensitive to changes in turns ratios, requiring careful design and optimisation through theoretical calculations. Additionally, proper design of the main switch snubber capacitor Cs is crucial to ensure soft-switching operation

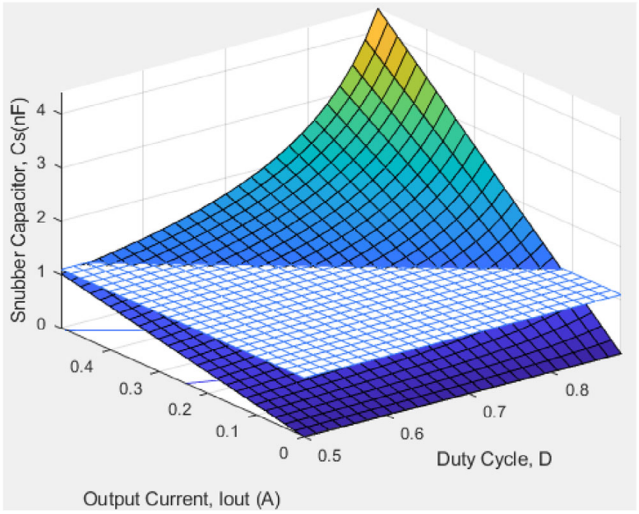



**FIGURE 8** | Maximum snubber capacitor to achieve ZVS as a function of duty cycle and output current.

even under worst-case conditions. This capacitor is specifically designed to regulate the overlap between the voltage and current of the switch at the turn-off moment. So, the snubber capacitor equations during turns-off and turn-on manners are obtained in Equations (36) and (37), respectively.

$$C_S \geq \frac{3GI_{out}t_f[1-D]}{2Y_v V_{in}} \tag{36}$$

$$\frac{1}{2}L_{lk2}{I_{Llk2}}^2 \geq \frac{1}{2}(C_{S1} \| C_{S2})(V_{C1}+V_{CC})^2 \tag{37}$$

The ZVS region for the main switch at the turn-off moment in the proposed converter is illustrated in Figure 8. The representation is three-dimensional, considering the duty cycle, output current, and the minimum snubber capacitor value necessary. The depicted surface at the base indicates the minimum snubber capacitance needed to ensure Zero Voltage Switching (ZVS) during turn-off. Figure 8 clearly demonstrates the extensive soft-switching range of the proposed converter for the chosen snubber capacitance.

In the next sections, a comprehensive comparison is done among the proposed converters and others in the literature review. Then, the control circuit and experimental results are presented, and the finally loss distribution is presented.

## 3.6 | Performance Comparison

In the comparison section, a detailed comparison is provided between the newly proposed high step-up boost converter and other existing high step-up topologies, and the results are reported in Table 4. Converters in [16, 18] require only one magnetic core, and they take advantage of the lowest component count, among others. However, they suffer from higher voltage stress of switches and diodes, low voltage gain and severe reverse recovery losses. Converters in [17] take advantage of the same soft-switching performance as [16, 18]. However, all of these converters suffer from capacitive turn-on loss, resulting in low efficiency. In terms of efficiency, the converter in [24] achieves the highest efficiency,

**TABLE 4** | Comparison of the proposed converter with other step-up boost converters.

| Converters | Soft switching cell | Voltage gain (G) | Duty cycle with n = 1, m = 0.1 and G = 13.33 | Switch voltage stress | Diode Voltage Stress | Efficiency in full load (%) | CIC* | CG* | Number of Components | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | MOS* | D | Cap | MC* | T* |
| Ref. [16] | Lossless Snubber-ZCS (on) | $\frac{1}{1-D}$ | 0.92 | $V_O$ | $V_O$ | 91 | ✓ | ✓ | 1 | 3 | 3 | 2 | 9 |
| Ref. [17] | | $\frac{2+n-D}{(1-D)(1-m)}$ | 0.81 | $\frac{V_O}{2+n-D}$ | $V_O - \frac{V_{in}}{(1-D)(1-m)}$ | 94.5 | ✓ | ✓ | 1 | 4 | 5 | 2 | 12 |
| Ref. [18] | | $\frac{1}{1-D}$ | 0.92 | $V_O$ | $V_O$ | 91 | ✓ | ✓ | 1 | 3 | 3 | 2 | 9 |
| Ref. [19] | ZVT | $\frac{2n+1}{1-2D}$ | 0.387 | $\frac{V_O}{2n+1}$ | – | 93.8 | × | × | 2 | 5 | 5 | 1 | 13 |
| Ref. [20] | | $\frac{n+2}{1-D}$ | 0.775 | $\frac{V_O}{n+2}$ | $\frac{(n+1)V_{in}}{(1-D)}$ | 97.6 | × | ✓ | 2 | 3 | 4 | 1 | 10 |
| Ref. [21] | | $\frac{n+2}{1-D}$ | 0.775 | $\frac{V_O}{n+2}$ | $\frac{2nV_O}{n+2}$ | 98.1 | × | ✓ | 4 | 3 | 4 | 2 | 13 |
| Ref. [22] | | $\frac{2+n_3D+n_2(1-D)}{1-2D}$ | 0.387 | $\frac{V_O}{2+n_3D+n_2(1-D)}$ | $\frac{V_O}{2+n_3D+n_2(1-D)}$ | 92 | ✓ | ✓ | 2 | 5 | 5 | 2 | 14 |
| Ref. [23] | Active clamp | $\frac{1+n}{1-D}$ | 0.845 | $\frac{V_O}{2(1+n)}$ | $\frac{V_O}{2}$ | 98 | × | × | 3 | 4 | 5 | 1 | 13 |
| Ref. [24] | | $\frac{2(1+n)}{1-D}$ | 0.7 | $\frac{V_O}{2(1+n)}$ | $\frac{V_O}{2(1+n)}$ | 98.15 | × | × | 2 | 4 | 5 | 1 | 13 |
| Ref. [25] | | G in [25] * | 0.7 | $V_{SW}$ in [25] * | $\frac{(1+m+n+mn)V_O}{2+m+n+mn+D(1+m)}$ | 97.5 | × | ✓ | 2 | 3 | 5 | 2 | 12 |
| Ref. [26] | | $\frac{2n(n+1)+4}{1-D}$ | 0.4 | $\frac{V_O}{2n(n+1)+4}$ | $\frac{V_O}{n(n+1)+2}$ | 95.3 | × | ✓ | 4 | 2 | 4 | 3 | 13 |
| Proposed converter | | $\frac{D(1+n)+(3+D)}{1-D}$ | 0.72 | $\frac{V_O}{D(1+n)+(3+D)}$ | $V_O-(1+D)\frac{V_{in}}{(1-D)}$ | 97.8 | ✓ | ✓ | 2 | 3 | 5 | 2 | 12 |

**Abbreviations: CIC:** Continuous Input Current; **C-G:** Common Ground, **MOS:** MOSFET; **D:** Diode; **Cap:** Capacitor; **MC:** Magnetic Components; **T:** Total. $G\ in\ [25] = \frac{2+m+n+mn+D(1+m)}{1-D}$ & $V_{SW}\ in\ [25] = \frac{V_O}{2+m+n+mn+D(1+m)}$.

**TABLE 5** | Power density and comparison cost of the proposed converter and converters in [20, 23, 25].

| Converters | Total Loss (W) | Efficiency in full load (%) | Power Density ($W/CM^3$) | Cost ($) |
|---|---|---|---|---|
| Ref. [20] | 4.9 | 97.6 | 1.12 | 13.65 |
| Ref. [23] | 4 | 98 | 0.82 | 19.54 |
| Ref. [25] | 5.16 | 97.5 | 0.85 | 15.36 |
| Proposed converter | 4.32 | 97.88 | 1.06 | 13.94 |

while the converter in [16] has the lowest efficiency among the others. Although the proposed converter has a lower efficiency compared to the converters in [21, 23, 24], it requires fewer components and features continuous input current.

From a soft-switching perspective, converters in [19–22] utilise a ZVT soft-switching condition which provides soft-switching range in a wide output power range. Among these converters, except for the converter in [22], the other ones suffer from discontinuous input current. In contrast, the proposed converter benefits from continuous input current, which is a significant feature for the proposed converter. Looking at the common ground feature, it can be seen that converters in [19, 23, 24] suffer from it.

The active clamp converters discussed in [23–26] exhibit load dependency and are unable to ensure a soft-switching condition under specific light loads. Furthermore, despite the converter in [26] suffering from a greater number of switches like the converter in [21] and having an inability to achieve a soft-switching condition under light loads, having a reduced number of diodes, high voltage gain, low switch voltage stress, and having a common ground are other remarkable advantages of this converter. In terms of component count, the proposed converter requires relatively fewer elements. In contrast, converters [19, 21–24, 26] employ a higher number of components, leading to a complex structure. Additionally, converters [16, 18, 20] consist of fewer elements, but they exhibit low voltage gain, high switch voltage stress and reverse recovery losses.

To sum up, while certain alternatives may feature higher voltage gain or a reduced number of elements, the proposed converter has achieved a balanced compromise across the desired parameters. Among the topologies which are shown in Table 4, the proposed converter stands out with its high voltage gain, continuous input current, soft switching performance in a wide range of output power and low stress voltage across the switch.

In addition, the proposed converter is compared with its main counterparts in terms of power density, efficiency and cost in Table 5. In addition, the power density of the proposed converter and its main counterparts are shown in Figures 9, 10, 11 and 12, respectively. As it can be seen, the proposed converter achieves a higher power density compared to the converters in [23, 25], while having a slightly lower power density than the converter in [20]. However, the converter in [20] suffers from discontinuous input current, lower voltage gain and efficiency, and higher costs compared to the proposed converter. In terms of cost, the converter in [20], having fewer components, is less expensive

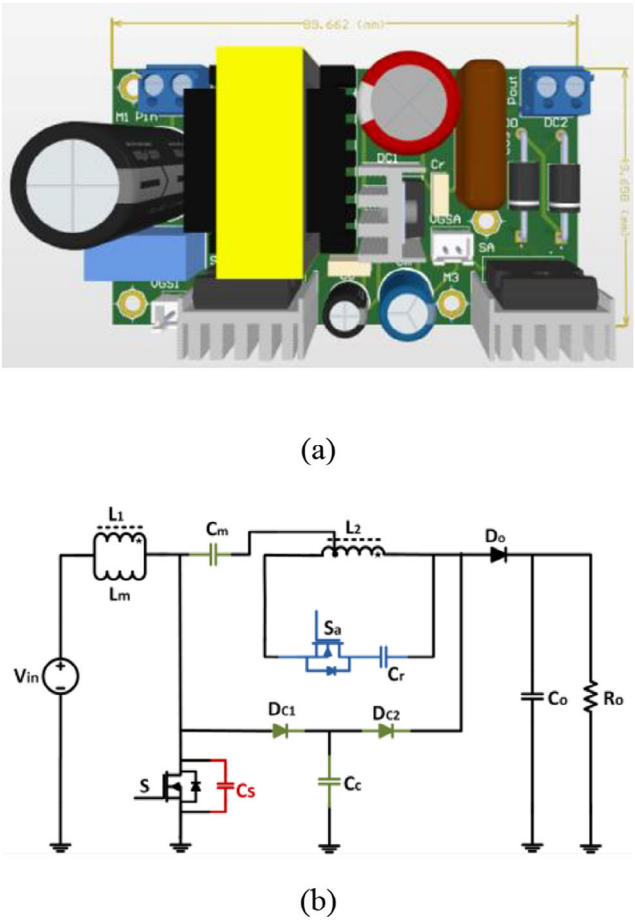



**FIGURE 9** | Prototype and schematic of the converter in [20].

than the proposed converter. However, in terms of efficiency, the proposed converter outperforms the converter in [20].

### 3.7 | Control Circuit and Experimental Results

The SG3526 IC was used to implement the closed-loop system, featuring dual PWM outputs, adjustable frequency, a built-in error amplifier with external RC filters for the PI controller, soft-start capability, overcurrent and overvoltage protection, synchronisation with an external clock, and adjustable dead time control. Additionally, two galvanically isolated gate drivers were used for enhanced noise immunity and extra protection, while isolated DC-DC converters enabled driving both the high-side and low-side switches. The schematic of the control circuit is shown in Figure 13.

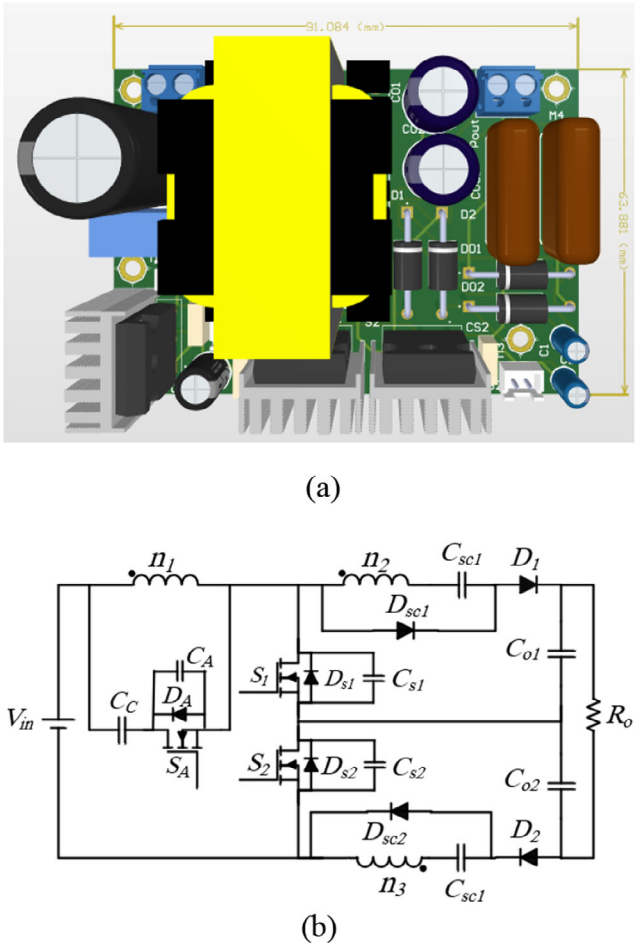



**FIGURE 10** | Prototype and schematic of the converter in [23].

To validate the effectiveness of the proposed converter, a laboratory prototype with an input voltage of 40 V, an output voltage of 400 V, and a rated power of 200 W has been implemented in real conditions. Figure 13 and Table 2 provide a comprehensive specification of the photograph and significant parameters of the implemented prototype, respectively. The experimental results of the introduced converter are depicted in Figure 14. Current and voltage waveforms of the main and auxiliary switches under full load conditions are presented in Figure 14a, b. As evident in these figures, both switches are turned on and turned off under ZVS performance, which reduced switching loss significantly. The drain-source voltage of $S_1$ and Sa are approximately 100 V, which is approximately a quarter of the output voltage. This enables the selection of low-voltage switches with smaller on-resistance, contributing to an improvement in efficiency. The voltage and current waveforms of $D_1$ and $D_2$ are depicted in Figure 14c, d. The maximum reverse voltage across $D_1$ is approximately 100 V, which is half of the $D_2$ voltage. As observed from $i_{D1}$ and $i_{D2}$, both diodes turn off under Zero Current Switching (ZCS) performance. As can be observed in Figure 14e, zero Current Switching (ZCS) conditions occur for the $D_O$ diode when this diode is turned off. The voltage stress across $D_O$ is half of the output voltage, and the presence of the leakage inductance contributes to reduced reverse recovery losses for the output diode. to display having soft switching performance in the light load, 20% nominal load, current and voltage waveforms of the main and auxiliary switches under light

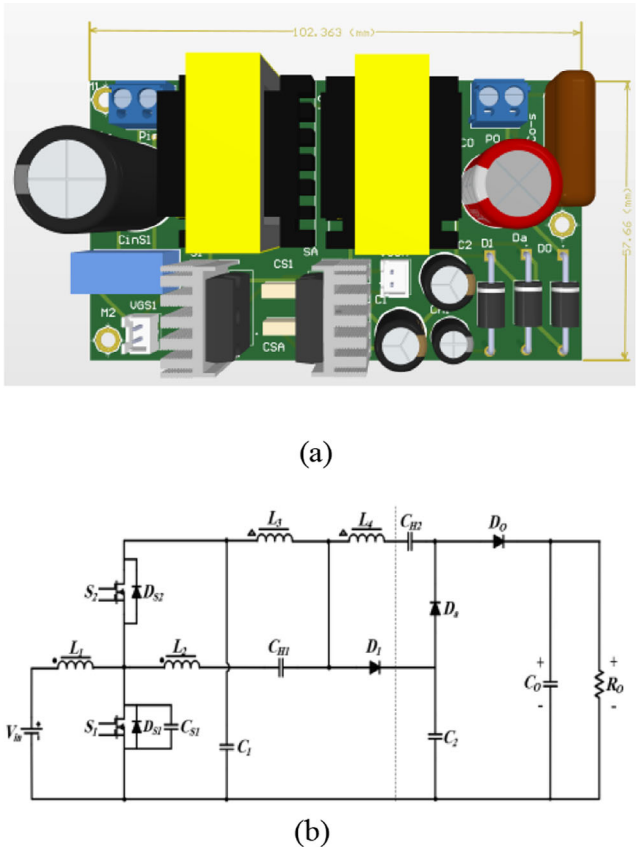
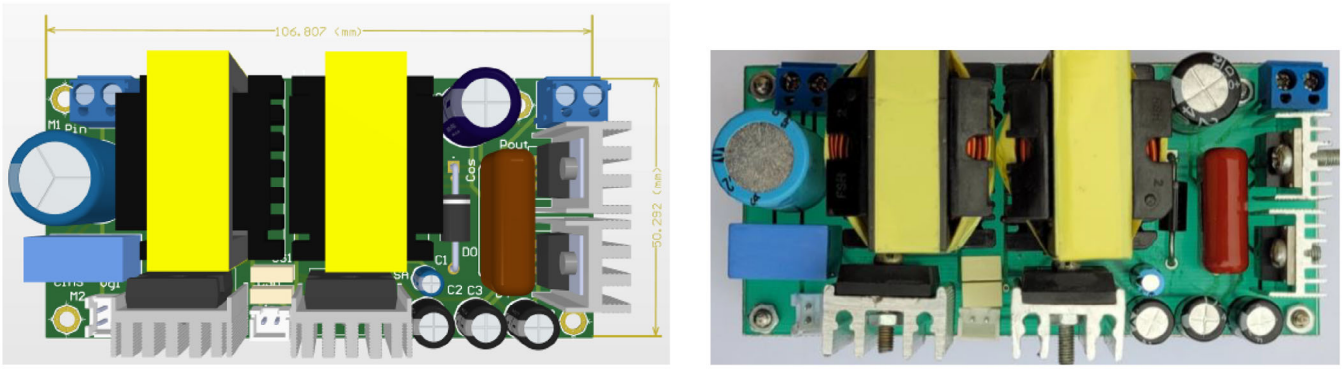



**FIGURE 11** | Prototype and schematic of the converter in [25].

load conditions are shown in Figure 14f, g. The input current waveform is illustrated in Figure 14h, where the input current remains continuous due to the presence of the input inductor. The low-ripple and continuous nature of the input current is a notable advantage of the proposed structure, especially when compared to step-up counterparts based on coupled inductors. This characteristic makes it a promising choice for applications in renewable energy and battery-based systems. The voltage of the $C_1$, $C_C$ and $C_2$ capacitors, as well as the $C_3$ capacitor is shown in Figure 14i–k. Finally, the transient response of the proposed converter is shown in Figure 14l. Also, simulation results of the proposed converter are shown in Figure 15.

## 4 | Loss Distribution and Efficiency

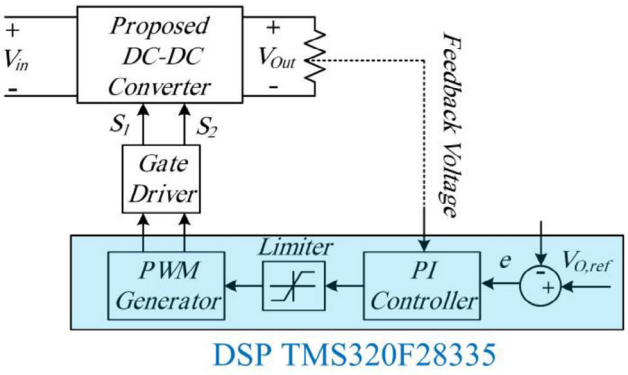
In this paper, a new single Given that one notable characteristic of the proposed converter is its utilisation of a small number of components, along with low losses at both full loads and light loads, it is essential to examine this particular feature. This section provides a comprehensive breakdown of losses for the proposed converter under both full load and light load conditions (50% of the nominal load). Additionally, two other ZVT and active clamp high step-up converters from references [20, 25] which have equal semiconductor elements are included for comparison (see Figure 16). Also, in this section, the simulation and analysis of the mentioned converters are conducted by using the OrCAD PSPICE software in the same situation according to Table 6. Within Figure 16, a detailed breakdown is provided for both the primary and auxiliary power components, which include power



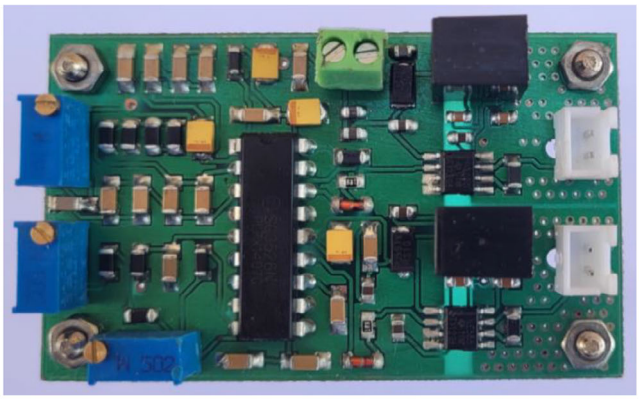

(a) 3D Prototype

(b) Implemented Prototype

**FIGURE 12** | PCB of the proposed circuit (a) 3d prototype (b) implemented prototype.




(a) Control Schematic



(b) Implemented Prototype

**FIGURE 13** | PCB of the proposed circuit (a) control schematic (b) implemented prototype.

switches, diodes, and inductors. Simultaneously, any additional losses associated with the gate driver and the equivalent series resistance (ESR) of capacitors are taken into account in the chart and labelled collectively as 'Others'. Also, the losses of the main switches encompass both conduction losses and switching losses during turn-off. This is due to the fact that achieving the zero-voltage switching (ZVS) condition at turn-off is facilitated by a snubber capacitor, and as a result, switching losses cannot be entirely eliminated. Since the auxiliary switch of the converter in [20] is turned on under ZCS performance, in addition to EOSS losses, EOSS losses are taken into account. Based on the

**TABLE 6** | Loss breakdown of all devices for the proposed converter.

| Component | Resistance [Ω] | RMS current [A] | Power loss [W] |
|---|---|---|---|
| Main switch | 0.0109 | 9.62 | 1 |
| Auxiliary switch | 0.0109 | 0.37 | 0.0015 |
| Inductor $L_{in}$ | 0.012 | 7.28 | 0.64 |
| Inductor $L_1$ | 0.003 | 6.5 | 0.126 |
| Inductor $L_2$ | 0.003 | 1.55 | 0.007 |
| **Component** | **Forward voltage [V]** | **Average current [A]** | **Power loss [W]** |
| Diode $D_1$ | 0.95 | 0.49 | 0.465 |
| Diode $D_2$ | 1.05 | 0.49 | 0.515 |
| Diode $D_O$ | 1.05 | 0.5 | 0.525 |
| Body diode of auxiliary switch | 0.95 | 0.58 | 0.55 |
| Total | | | 3.82 |

information from Figure 16, it is evident that the losses of the $D_1$ and $D_O$ diodes in full load for converters in [20, 25] are exactly equal. Also, the losses of the main switch for converters in [20, 25] show the highest value, remarkably contributing to the overall losses. Moreover, the losses associated with the main switch in the proposed converter are lower compared to the converters in [20, 25]. This reduction in losses is attributed to the utilisation of switch lower RDS-on, resulting in lower conduction losses in the proposed topology. The impact of loss in main and auxiliary switches becomes more notable at the proposed converter, and it stands out as a key factor contributing to the high efficiency observed under these conditions. Although winding losses of full and light loads in the proposed converter are more than its counterparts, the proposed converter takes advantage of continuous input current that converters in [20, 25]. Table 6 provides a comprehensive breakdown of conduction loss calculations for the proposed converter at nominal load, encompassing losses in switches, diodes, and windings.

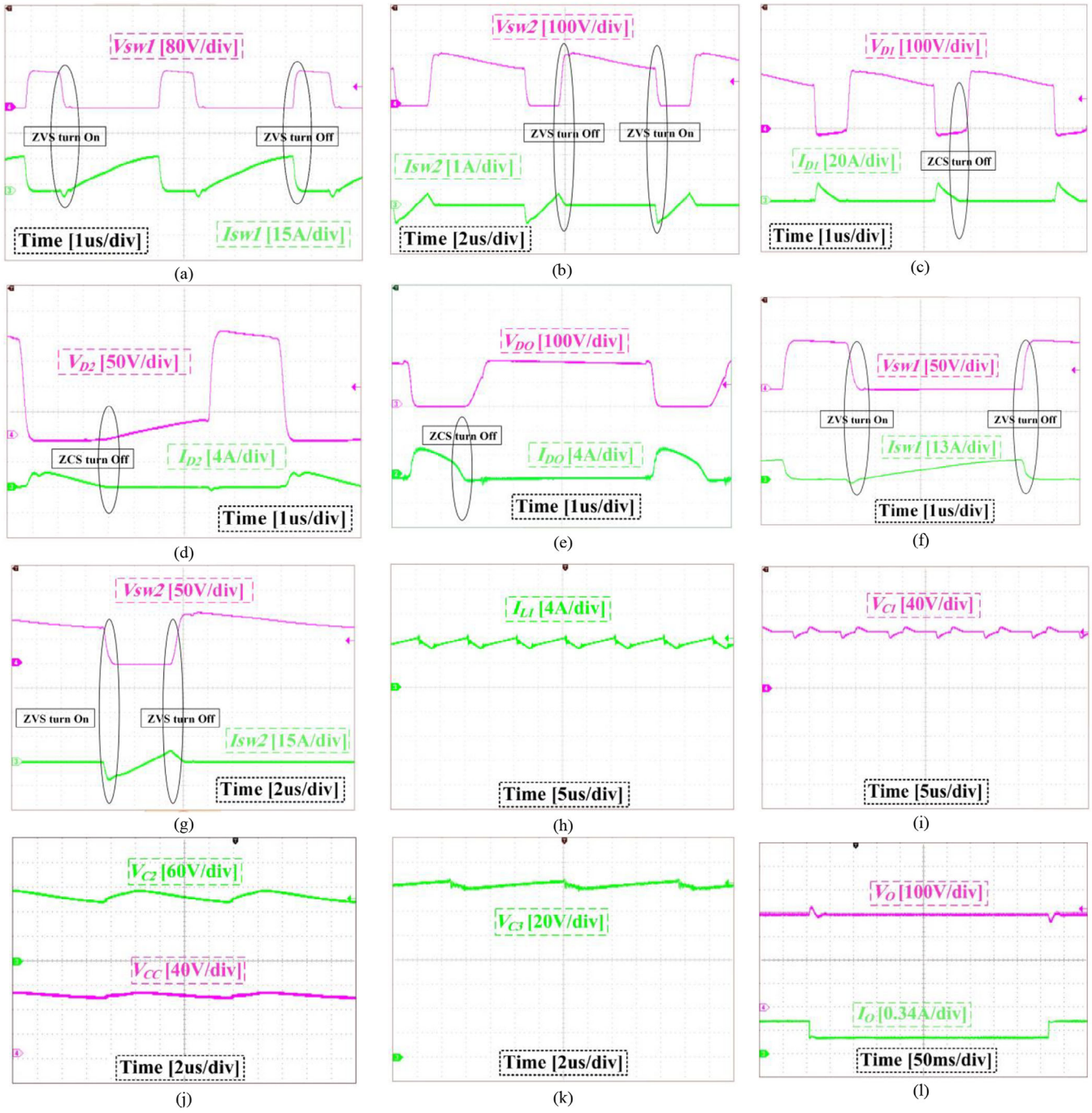



**FIGURE 14** | Experimental waveforms of the implemented prototype, (a) $V_{DS1}$, $I_{DS1}$, (b) $V_{DS2}$, $I_{DS2}$, (c) $V_{D1}$, $I_{D1}$, (d) $V_{D2}$, $I_{D2}$ (e) $V_{DO}$, $I_{DO}$ (f) $V_{DS1}$, $I_{DS1}$ at light load, (g) $V_{DS2}$, $I_{DS2}$ at light load (h) $I_{L1}$, (i) voltage of $C_1$ capacitor, (j) voltage of $C_2$ and $C_C$ capacitor, (k) voltage of $C_3$ capacitor, (l) transient response.

For evaluating efficiency, the proposed converter is compared with references in [20, 25] by utilising computer simulations performed with PSpice software, results which are shown in Figure 17. As it can be observed in Figure 17, The proposed converter demonstrates the highest full-load efficiency, reaching 97.8% in the simulation at 200 W output power. Furthermore, there is negligible efficiency decline between the proposed converter and [20] at light loads. Unlike the converter in [20], the proposed converter exhibits continuous input current and a higher voltage gain. While the converter in [25] achieves high efficiency at light loads, it also experiences discontinuous input current, contrasting with the continuous operation of the proposed converter.

## 5 | Conclusion

In this paper, a soft-switched high step-up DC-DC converter is introduced in, which by using coupled inductor and switched

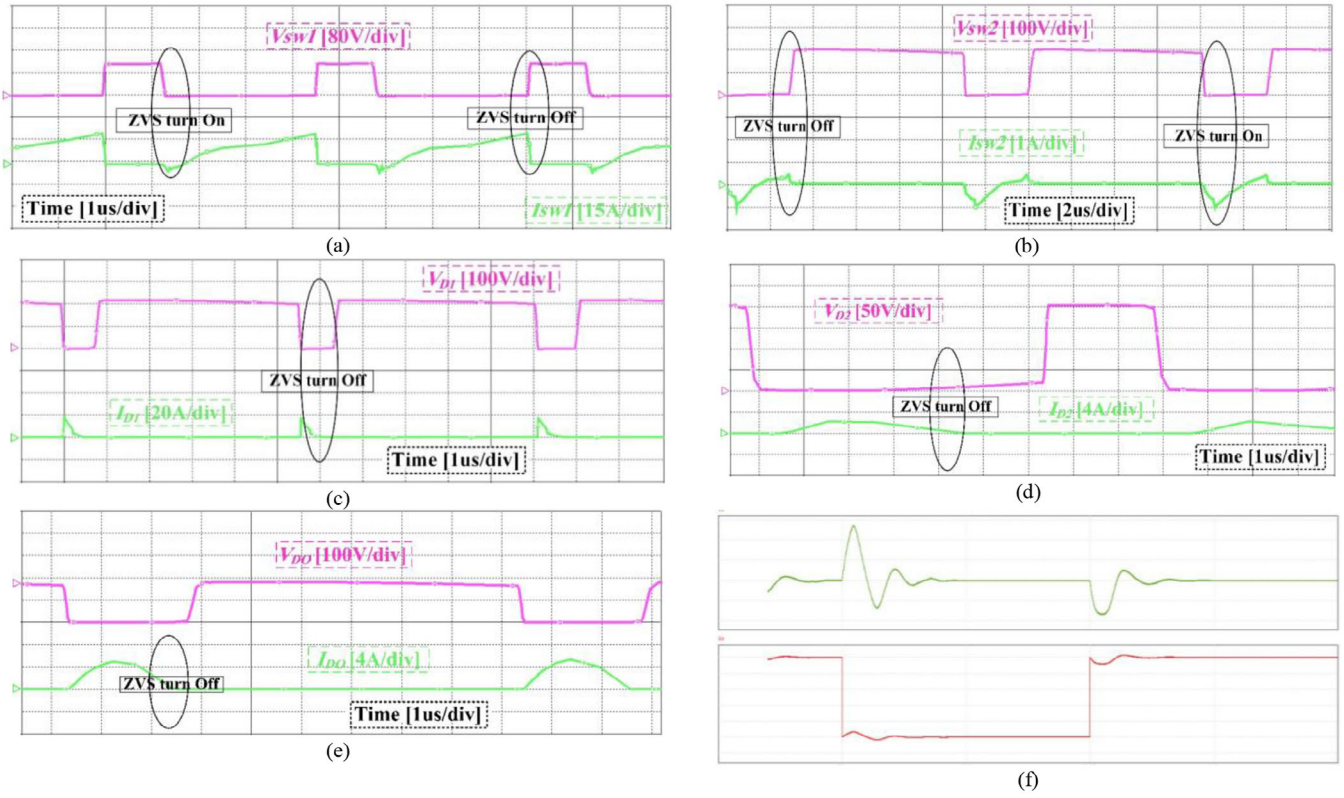



**FIGURE 15** | Simulation waveforms of the implemented prototype, (a) $V_{DS1}, I_{DS1}$, (b) $V_{DS2}, I_{DS2}$, (c) $V_{D1}, I_{D1}$, (d) $V_{D2}, I_{D2}$ (e) $V_{DO}, I_{DO}$ (f) transient response.

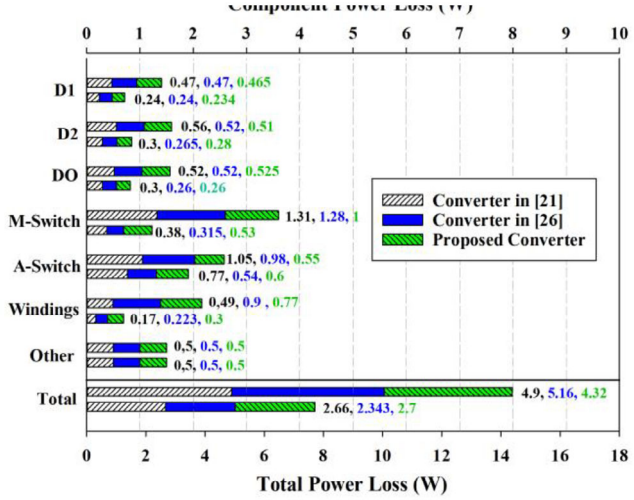



**FIGURE 16** | Losses breakdown of the proposed converter, converters in [20, 25].

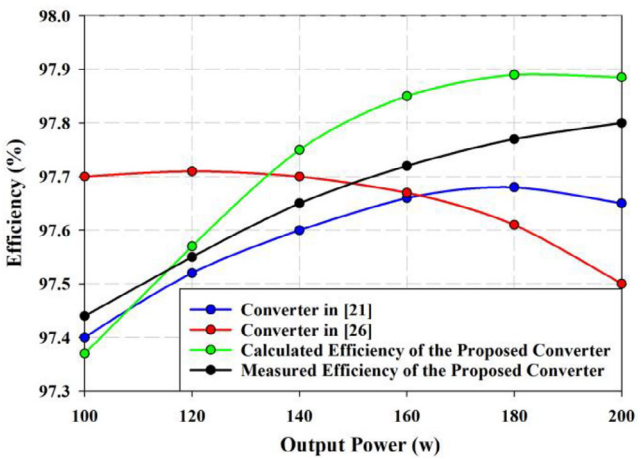



**FIGURE 17** | Measured and Calculated Efficiency of the proposed converter in comparison with converters in [20, 25].

capacitor techniques, high voltage gain is obtained. In the proposed converter, the voltage stress across the main and auxiliary switches is limited to less than a quarter of the 400 V output voltage, which cause use switches with low RDS-ON, resulting in low losses and high efficiency. Also, since the active clamp technique is used in this converter, soft-switching performance is achieved in this converter, leading to achieving a full load efficiency of 97.8%. In addition, the proposed converter takes advantage of a continuous input current, made possible by the presence of the input inductor. This feature proves especially beneficial in renewable energy applications and enables the use of smaller input filter capacitors. The proposed converter has been designed with an input voltage of 30 V, an output voltage of 400 V, an output power of 200 W, and a switching frequency of 100 kHz. Additionally, the voltage stress across the main switch is approximately one-fourth of the output voltage.

### Author Contributions

**Sadegh Heidari Beni:** conceptualisation, investigation, software, writing – original draft. **Sayyed Mohammad Mehdi Mirtalaei:** supervision, validation, writing – review and editing. **Mahdi Shaneh:** supervision, validation, writing – review and editing. **Tohid Nouri:** supervision, validation, writing – review and editing. **Amir Baktash:** supervision, validation, writing – review and editing.

### Conflicts of Interest

The authors declare no conflicts of interest.

### Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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