In The Name of Almighty

Lec. 4:
Flash ADC (Part-I)
Architecture & Challenges

Lecturer: Samaneh Babayan
Integrated Circuit Lab.
Department of Computer Science & Engineering
ImamReza University of Mashhad
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Lecturer: Hooman Farkhani
Department of Electrical Engineering
Islamic Azad University of Najafabad
Email: H_farkhani@yahoo.com
Analog to Digital Converters

- **Nyquist-Rate ADCs**
  - Flash ADCs
  - Sub-Ranging ADCs
  - Folding/ Interpolating ADCs
  - Pipelined ADCs
  - Successive Approximation ADCs (SA-ADCs)
  - Integrating (serial) ADCs

- **Oversampling ADCs**
  - Delta-Sigma based ADCs
Nyquist ADC Architectures

- Nyquist rate
  - Word-at-a-time
    - E.g. flash ADC
    - Instantaneous comparison with $2^B-1$ reference levels
  - Multi-step
    - E.g. pipeline ADCs
    - Coarse conversion, followed by fine conversion of residuum
  - Bit-at-a-time
    - E.g. successive approximation ADCs
    - Conversion via a binary search algorithm
  - Level-at-a-time
    - E.g. single or dual slope ADCs
    - Input is converted by measuring the time it takes to charge/discharge a capacitor from/to input voltage
## Conversion Principles

<table>
<thead>
<tr>
<th>Principle</th>
<th>Resolution</th>
<th>Speed</th>
<th>Cost</th>
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<tbody>
<tr>
<td>Serial Conversion</td>
<td>High &gt;12 Bit</td>
<td>Low &lt;1kHz</td>
<td>Low</td>
</tr>
<tr>
<td>Successive Approximation</td>
<td>Medium 8-14 Bit</td>
<td>Medium &lt;100MHz</td>
<td>Medium</td>
</tr>
<tr>
<td>Parallel Conversion</td>
<td>Low 6-10 Bit</td>
<td>High &gt;100MHz</td>
<td>High</td>
</tr>
<tr>
<td>Delta Sigma</td>
<td>High &gt;12 Bit</td>
<td>Low-Medium &lt;1MHz</td>
<td>Low (analog only)</td>
</tr>
</tbody>
</table>
ADC Architectures

- **Flash ADCs:**
  - High speed, but large area and high power dissipation. Suitable for low-medium resolution (6-10 bit).

- **Sub-Ranging ADCs:**
  - Require exponentially fewer comparators than Flash ADCs. Hence, they consume less silicon area and less power.

- **Pipelined ADCs:**
  - Medium-high resolution with good speed. The trade-offs are latency and power.

- **Successive Approximation ADCs:**
  - Moderate speed with medium-high resolution (8-14 bit). Compact implementation.

- **Integrating ADCs or Ramp ADCs:**
  - Low speed but high resolution. Simple circuitry.

- **Delta-Sigma based ADCs:**
  - Moderate bandwidth due to oversampling, but very high resolution thanks to oversampling and noise shaping.
ADC Architectures
Flash ADC Speed

![Graph showing the clock speed of Flash ADCs and microprocessors over years from 1996 to 2008. The graph indicates an increase in clock speed over time, with Flash ADCs generally outpacing microprocessors.]
Flash ADC

• **Advantages**
  1. Conceptually most straightforward
     One clock cycle / conversion
     highest possible speed
  2. resolution: 3 ~ 8 bits
  3. clock rates 20 MHz ~ tens of GHz

• **Disadvantages:**
  1. \((2^N - 1)\) comparators required
     Hardware complexity grows exponentially with resolution
  2. Comparator offset limit the resolution
  3. Large Power Consumption
  4. Complex Layout Issues
Flash ADC

Thermometer Code

\( V_{FS} \) \( V_i \) Strobe \( f_s \) 0 1

\( 2^{N-1} \) comparators

1-of-n code

ROM encoder

Thermometer code

1

0

1

0

1

b_2 \ b_1 \ b_0

111

110

010

001

000

V_{FS} \ V_i \ f_s \ b_2 \ b_1 \ b_0 \ 2^{N-1} \ \text{comparators} \ 1\text{-of-}n \ \text{code} \ \text{ROM} \ \text{encoder}
Flash ADC Challenges

- High Complexity ($2^N-1$ Comparators):
  - consumes large area
  - high input capacitor
  - Large power consumption
  - Large comparators needed for removing offset.
- Limited to the resolution of 4-8 Bits.
- Speed limited by single comparator plus encoding logic.

- $V_{DD} = 1.8$ V
- 10-bit
- $V_{FS} = 1$ V
- DNL $< 0.5$ LSB
- $0.5$ mV $= 3$-$5$ $\sigma$

$\rightarrow$ 1023 comparators
$\rightarrow$ 1 LSB $= 1$ mV
$\rightarrow$ $V_{os} < 0.5$ LSB
$\rightarrow$ $\sigma = 0.1$–$0.2$ mV
Flash ADC Challenges

- DNL < 0.5 LSB
- Large $V_{FS}$ relaxes offset tolerance
- Small $V_{FS}$ benefits conversion speed
  - (settling, linearity of building blocks)

![Graph showing $V_{os, max}$ vs $N$ for different $V_{FS}$ values.](chart.png)

$V_{FS} = 1V$
$V_{FS} = 2V$

$f_{os, max}$ [mV]

$N$ [bits]
A Typical CMOS Comparator

$V_{os}$ derives from:
- Preamp input pair mismatch ($V_{th}, W, L$)
- PMOS loads and current mirror
- Latch mismatch
- CI / CF imbalance of $M_9$
- Clock routing
- Parasitics
Exponential regeneration due to positive feedback of $M_7$ and $M_8$
Regeneration Speed – Linear Model

\[ \begin{align*}
V_o^+ &= -V_o^- \\
V_o^+ &= -g_m \cdot V_o^- / sC_L
\end{align*} \]

\[ \begin{pmatrix} 1 & 1 \\ 1 & g_m / sC_L \end{pmatrix} \begin{pmatrix} V_o^+ \\ V_o^- \end{pmatrix} = 0 \]

\[ \Delta(s) = g_m / sC_L - 1 = 0 \Rightarrow s_p = g_m / C_L, \text{ single RHP pole} \]

\[ V_o(t > 0) = V_o(t = 0) \cdot \exp(t \cdot g_m / C_L) \]
Reg. Speed – Linear Model

\[
V_o(t=0) = \frac{C_L}{g_m} \cdot \ln \left( \frac{V_o(t)}{V_o(t=0)} \right)
\]

<table>
<thead>
<tr>
<th>( V_o )</th>
<th>( V_o(t=0) )</th>
<th>( t/(C_L/g_m) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1V</td>
<td>100mV</td>
<td>2.3</td>
</tr>
<tr>
<td>1V</td>
<td>10mV</td>
<td>4.6</td>
</tr>
<tr>
<td>1V</td>
<td>1mV</td>
<td>6.9</td>
</tr>
<tr>
<td>1V</td>
<td>100( \mu )V</td>
<td>9.2</td>
</tr>
</tbody>
</table>
Reg. Speed – Linear Model

\[ |A_{V1}| = \frac{g_{m1}}{g_{m3}} \]

\[ |A_{V2}| = \frac{g_{m5}R_9}{2 - g_{m7}R_9}, \quad \frac{R_9}{2} < \frac{1}{g_{m7}} \]

to be amplifier.

\[ V_o(0) = V_i(0) \cdot A_V = V_i(0) \cdot A_{V1}A_{V2} \]

\[ V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L) \]
Comparator Metastability

Comparator fails to produce valid logic outputs within $T/2$ when input falls into a region that is sufficiently close to the comparator threshold.

$$V_o(t) = V_i(0) \cdot A_{V1} A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

<table>
<thead>
<tr>
<th>Curve</th>
<th>$A_{V1}A_{V2}$</th>
<th>$V_i(t=0)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>10 mV</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>1 mV</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>100 $\mu$V</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>10 $\mu$V</td>
</tr>
</tbody>
</table>
Comparator Metastability

- Cascade preamp stages (typical flash comparator has 2–3 PA stages)
- Use pipelined multi-stage latches; PA can be pipelined too
- Avoid branching off comparator logic outputs

Assuming that the input is uniformly distributed over $V_{FS}$, then

$$\text{BER} = \frac{\Delta}{1 \text{ LSB}}$$

$$V_o(t) = V_i(0) \cdot A_{V1} A_{V2} \cdot \exp(t \cdot g_m / C_L)$$
Logic levels can be misinterpreted by digital gates (branching off, diff. outputs) – even a wrong decision is better than no decision!
Charge injection and clock feedthrough introduce CM jump in $V_o^+$ and $V_o^-$. Dynamic latches are more susceptible to CI and CF errors.
Dynamic Offset of Latch

Dynamic offset derives from:

- Imbalanced CI and CF
- Imbalanced load capacitance
- Mismatch b/t M₇ and M₈
- Mismatch b/t M₅ and M₆
- Clock routing

0.5V CM jump
10% imbalance \( \implies \) 50mV offset

Dynamic offset is usually the dominant offset error in latches
Typical CMOS Comparator

- Input-referred latch offset gets divided by the gain of PA
- Preamp introduces its own offset (mostly static due to $V_{th}$, $W$, and $L$ mismatches)
- PA also reduces kickback noise

Kickback noise disturbs reference voltages, must settle before next sample
Comparator Offset

Differential pair mismatch:

\[
V_{os}^2 = (\Delta V_{th})^2 + \frac{1}{4} V_{ov}^2 \left[ \left( \frac{\Delta W}{W} \right)^2 + \left( \frac{\Delta L}{L} \right)^2 \right]
\]

\[
|A_{V1}| = \frac{g_{m1}}{g_{m3}} \quad |A_{V2}| = \frac{g_{m5}R_9}{2 - g_{m7}R_9}
\]

Total input-referred comparator offset:

\[
V_{os}^2 = V_{os,12}^2 + \frac{V_{os,34}^2}{A_{V1}^2} + \frac{V_{os,56}^2}{A_{V1}^2 A_{V2}} + \frac{V_{os,78}^2}{A_{V1}^2 A_{V2}^2} + \frac{V_{os,dyn}^2}{A_{V1}^2 A_{V2}^2}
\]
Matching Properties

Suppose parameter $P$ of two rectangular devices has a mismatch error of $\Delta P$. The variance of parameter $\Delta P$ b/t the two devices is

$$
\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2,
$$

where, $W$ and $L$ are the effective width and length, $D$ is the distance.

1st term dominates for small devices.

Threshold: $\sigma^2(V_{th}) = \frac{A_{V_{th}}^2}{WL} + S_{V_{th}}^2 D^2$

Current factor: $\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_{\beta}^2}{WL} + S_{\beta}^2 D^2$

Why Large Devices Match Better?

\[ R_1 = R_S \cdot \frac{L}{W} \] with std \( \sigma_{R_1} \)

\[ R_2 = R_S \cdot 10 \left( \frac{L}{W} \right) = 10R_1 \] with std \( \sigma_{R_2} \),

\[ \sigma_{R_2}^2 = \sum_{j=1}^{10} \sigma_{R_j}^2 = 10\sigma_{R_1}^2 \Rightarrow \sigma_{R_2} = \sqrt{10}\sigma_{R_1} \]

\[ \frac{\sigma_{R_2}}{R_2} = \frac{\sqrt{10}\sigma_{R_1}}{10R_1} = \frac{1}{\sqrt{10}} \left( \frac{\sigma_{R_1}}{R_1} \right) \Rightarrow \frac{\sigma_R}{R} \propto \frac{1}{\sqrt{A}} = \frac{1}{\sqrt{WL}} \]

"Spatial averaging"
**ADC Input Capacitance**

\[ \sigma^2 (V_{th}) = \frac{A_{vth}^2}{WL} \quad C_g = 10 \text{ fF} / \mu m^2 \]

- **N = 6 bits** → 63 comparators
- **\( V_{FS} = 1 \text{ V} \)** → 1 LSB = 16 mV
- **\( \sigma = \text{LSB}/4 \)** → \( \sigma = 4 \text{ mV} \)
- **\( A_{VT0} = 10 \text{ mV} \cdot \mu m \)** → \( L = 0.24 \mu m, \ W = 26 \mu m \)

<table>
<thead>
<tr>
<th>N (bits)</th>
<th># of comp.</th>
<th>( C_{in} ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>63</td>
<td>3.9</td>
</tr>
<tr>
<td>8</td>
<td>255</td>
<td>250</td>
</tr>
<tr>
<td>10</td>
<td>1023</td>
<td>??!</td>
</tr>
</tbody>
</table>

- Small \( V_{os} \) leads to large device sizes, hence large area and power
- Large comparator leads to large input capacitance, difficult to drive and difficult to maintain tracking bandwidth
References

- Professor Boris Murmann Course slides 2012, Stanford University- EE315B course
- Dr. Reza Lotfi, ADC course slides 2008