scientific reports

OPEN

A new ultra-high voltage gain DC/DC converter based on coupled-inductor

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In this paper, a new ultra-high voltage gain quadratic DC-DC converter based on coupled-inductor is introduced for renewable energy applications. In this presented topology, a two-winding coupled-inductor along with voltage multiplier cells are combined with a quadratic boost converter to enhance the voltage gain ratio. The main features of the suggested converter are its ultra-high voltage conversion ratio, low voltage stress across switching devices, continuous input current with low ripple, and common ground between the input source and output sides. Moreover, the current sharing of the high DC source current between the coupled-inductor and another input inductor leads to the reduction of the overall power losses of the magnetic components of this circuit. Furthermore, the voltage maximum stresses on the switches of this converter are mitigated with the help of regenerative passive clamp circuits. The operating principle, the steady-state DC analysis, comparison study along with the efficiency analysis of the introduced topology are presented in detail. Finally, the performance of the proposed converter is justified with the help of a 200 W (25 V-400 V) laboratory sample prototype.

To produce power in clean and pollution-free conditions, Renewable Energy Sources (RES) such as fuel cells and photovoltaics would be the vital solution. However, because of low DC voltage (< 50 V), a high step-up (high-voltage gain) DC-DC converter is essential as an interface device to procure the optimal energy from RES[1,2]. Moreover, some other applications of high step-up DC-DC topologies are in lighting systems, medical devices, energy harvesting, uninterruptible power supply (UPS), and portable devices[2]. To satisfy the optimum power transfer from renewable energy sources, a high voltage gain converter with a low input current is required[3]. For this purpose, most of the switched-mode converters that are used to increase the DC voltage are current-fed strategy type. In addition, high voltage gain, low voltage stress accross the switching devices, enough high efficiency, and low component count are the other key performance indicators of the high step-up converters[2,3]. Also, non-isolated step-up DC-DC structures with low component counts are often preferred for low power applications[2].

So far, many DC-DC structures with high step-up structures have been introduced to provide high-output DC voltage from low-voltage RESs. In these circuits, in order to create the voltage gain, some typical voltage-boosting methods including voltage lift, switched inductor (SI), switched capacitor (SC), cascading method, interleaved technique, and also voltage multiplier (VM) cells have been applied[4–8]. Nonetheless, for high voltage gain applications, utilizing a large number of components in the circuit, and hard-switching conditions are the main demerits of most of these topologies, which limits their application[9,10]. By combining voltage boosting methods (SC, SI, and VM) with magnetic devices (Coupled-Inductor (CI) and transformer), better performance indicators can be obtained for a high step-up DC-DC converters[11,12]. However, in CI-based structures, using an active or passive clamp circuit is necessary to restrict the high voltage stresses on the power switch, which is imposed by the leakage inductance of the CI[3,13].

The quadratic structure is a type of high step-up DC-DC converter that has the ability to create high voltage gains under a low number of components. In such circuits, the voltage gain is an exponential function of the duty-cycle of the converter. In recent years, many non-isolated modified structures of the quadratic converters with proper key performance indicators have been presented. In[9,10], two types of transformer-less high step-up quadratic DC/DC converter for low power applications are presented. However, these topologies are able to create high voltage conversion ratios with the help of a large number of components.

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Recently, a large number of quadratic converters based on CIs have been presented. Two new quadratic high step-up DC-DC converters based on CI and VMs with low voltage stress are suggested in[14,15]. Although very high voltage gains, these topologies suffer from high input current ripple, which limits their applications for RES. To solve this problem, in[16–18], single-switch CI-based DC-DC structures with quadratic voltage gain ratio and low input current ripple are introduced. Nevertheless, in these circuits, the power dissipation in the input diodes of the converter is considerable. Besides, three new structures of high voltage gain quadratic DC-DC converters with low voltage stress are proposed in[19–21]. However, in the mentioned topologies, because of the series connection between the CI and input source, input current with large ripple is imposed on the input DC source. In[22–24], by combination of a three-winding coupled-inductor (TWCI) and VM cells, several high step-up quadratic converters with a low input current ripple are suggested. In such circuits, it is possible to obtain high voltage gains using more degrees of freedom. Nevertheless, these converters suffer from high voltage stress across the power switch and high-power losses for the input diodes. Also, in[25], a new quadratic double-switch DC-DC converter is introduced composed of two stages boost converter, CI and VM. In this circuit, due to the current sharing between the CI and input inductor, the power losses of the magnetic devices are low. Nonetheless, in this topology, a high component count is utilized to create high voltage gains. Furthermore, a new double-switch high voltage gain quadratic converter with continuous input current and low switch voltage stress is presented in[26]. However, low voltage gain ratio is the main disadvantages of the mentioned circuit. In[27–30]some modified single-switch high voltage gain quadratic DC-DC topologies based on TWCI with low input current are presented. Nevertheless, the lack of common ground between the input side and output DC load is the main demerits of the mentioned circuits. Also, three new high voltage gain with partial trans-inverse feature have been proposed in[31,32]. However, high voltage stress on the power switch and high average current values of the input diodes are considered as disadvantages of these circuits. Moreover, a new TWCI-based high voltage gain DC-DC converter with common ground and low input current ripple has been presented in[33]. However, the steep slope of voltage gain in this topology makes the control procedure more complex. In addition, recently, a new modified bipolar high-gain DC-DC converter with low input current ripple and partial trans-inverse specification is suggested in[34]. However, limitation in voltage gain is the main disadvantages of this topology. Moreover, in[35,36], two new types of interleaved DC-DC converters based on CI have been introduced. However, in these converters, ultra-high voltage gain is achieved by using a large number of components. New single-switch high voltage gain DC-DC converters using a three winding CI with trans-inverse feature are also proposed in[37,38]. Nevertheless, these converters suffer from high current levels in the magnetic devices and power switches. In addition, in[39] a Z-source DC-DC structure with high voltage gain and low input current ripple is introduced. However, in this converter, the duty cycle range is limited and the steep slope of voltage gain makes the control very sensitive to the presence of any disturbance such as load variation.

Motivated by discussed topologies, this paper introduces a new modified quadratic high step-up DC-DC converter for RES applications. The advantages of the proposed topology are as follows:

1-Ultra-high voltage gain ratio.
2-Low component counts.
3-Continuous input current with low ripple.
4-Low voltage stress on the switching components.
5-Common ground between input DC source and output load.
6-Low current stress for the switches and magnetic devices.

This paper is organized as follows: Operational principles of the presented topology along with its comprehensive analysis are investigated in detail in Sections II and III. In Section IV, the key indicators of the introduced circuit are also compared with similar counterparts. Moreover, the small signal modelling of the proposed circuit is provided in section V. The experimental results are provided in Sections VI that is followed by conclusions in section VII.

Proposed converter and operating principles

Figure 1 demonstrates the circuit schematic of the proposed converter. It consists of two power MOSFETs S_1, S_2; five diodes D_1, D_2, D_3, D_4, D_5; five capacitors C_1, C_2,C_3,C_4,C_O; a discrete inductor L_1; a two-winding CI in which L_K is the leakage inductor and L_M represents its magnetizing inductor. V_{in} and I_{in} symbolize the input voltage and current; V_O and I_O notate the output voltage and current and R_o is the resistance of the load. N_1 and

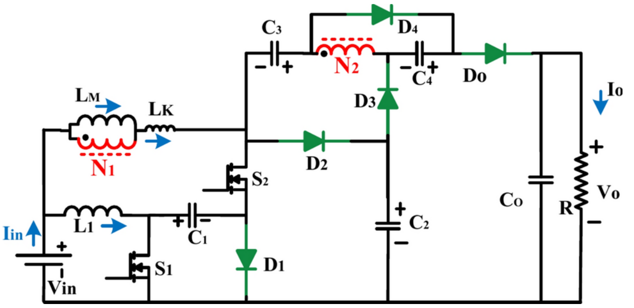


Fig. 1. Circuit schematic of the proposed converter.

N_2 are the number of the turns of the primary and secondary windings of the CI and the turns ratio is defined as $n = N_2/N_1$. Power MOSFETs are switched ON and OFF simultaneously with the same duty cycle D. Note that:

- L_{in} is large enough to maintain its passing current continuous.

- The converter operates in continuous conduction mode (CCM) when i_{LM} is continuous while it operates in dis-continuous conduction mode (DCM) for dis-continuous i_{LM}. Moreover, the boundary conduction mode (BCM) is defined as the boundary of CCM and DCM.

A. CCM operation

The Key waveforms and the equivalent circuits of the proposed converter during a switching cycle are illustrated in Fig. 2 and Fig. 3, respectively. There are eight modes of operation in a switching cycle that are discussed as follows.

Mode I $[t_0 \sim t_1]$: The equivalent circuit of this mode is shown in Fig. 3(a). At time t_0, the power MOSFETs are turned ON and the ZCS turn ON is provided for S_2. The diode D_1 is reverse biased by the voltage of V_{C1} and turns OFF. The inductors L_1 and L_M start charging by V_{in} and $V_{in} + V_{C1}$, respectively. The residue energy of the leakage inductor is delivering to the load through diode D_O, during this time interval. At time t_1, the passing current of D_O reaches to zero and turns OFF with ZCS performance. As a result, the reverse recovery is alleviated.

$$\frac{di_{DO}}{dt} = \frac{V_{C3} + V_{C4} - (n+1)\,V_{C1} - nV_{in} - V_O}{n^2 L_K} \tag{1}$$

Mode II $[t_1 \sim t_2]$: The equivalent circuit of this mode is shown in Fig. 3(b). At time t_1, diode D_3 is turned ON. Capacitors C_1, C_2 and C_3 are discharging and charging, as well. The output load is supplied by capacitor C_O. The passing current through the MOSFETs are given by:

$$i_{S1} = i_{L1} + i_{LM} + (n+1)\,i_{D3} \tag{2}$$

$$i_{S2} = i_{LM} + (n+1)\,i_{D3} \tag{3}$$

At time t_2, D_4 is turned ON and this time interval ends.

Mode III $[t_2 \sim t_3]$: The equivalent circuit of this mode is shown in Fig. 3(c). During this mode, some part of he absorbed energy from the input power source is delivering to the capacitor C_4 and the passing currents through D_3 and D_3 are decreasing and increasing, respectively. The currents of the switches are obtained as:

$$i_{S1} = i_{L1} + i_{LM} + (n+1)\,i_{D3} + ni_{D4} \tag{4}$$

$$i_{S2} = i_{LM} + (n+1)\,i_{D3} + ni_{D4} \tag{5}$$

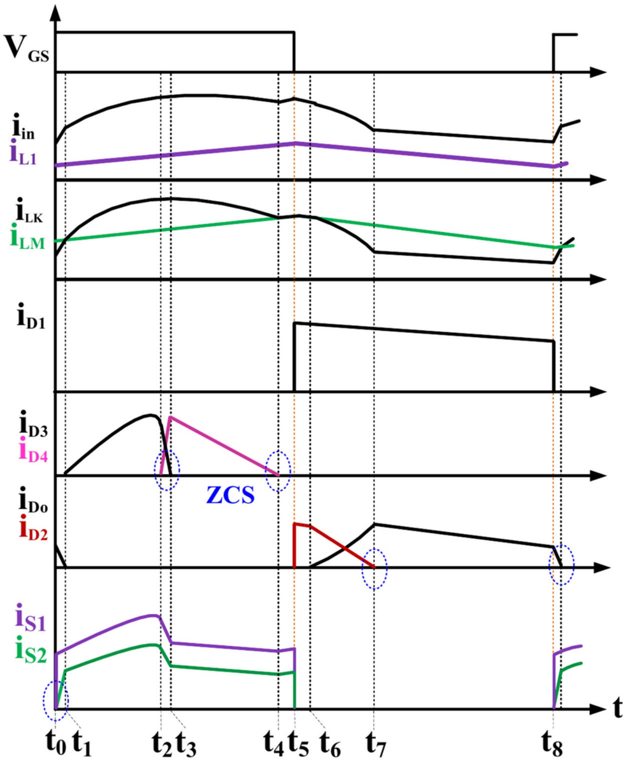
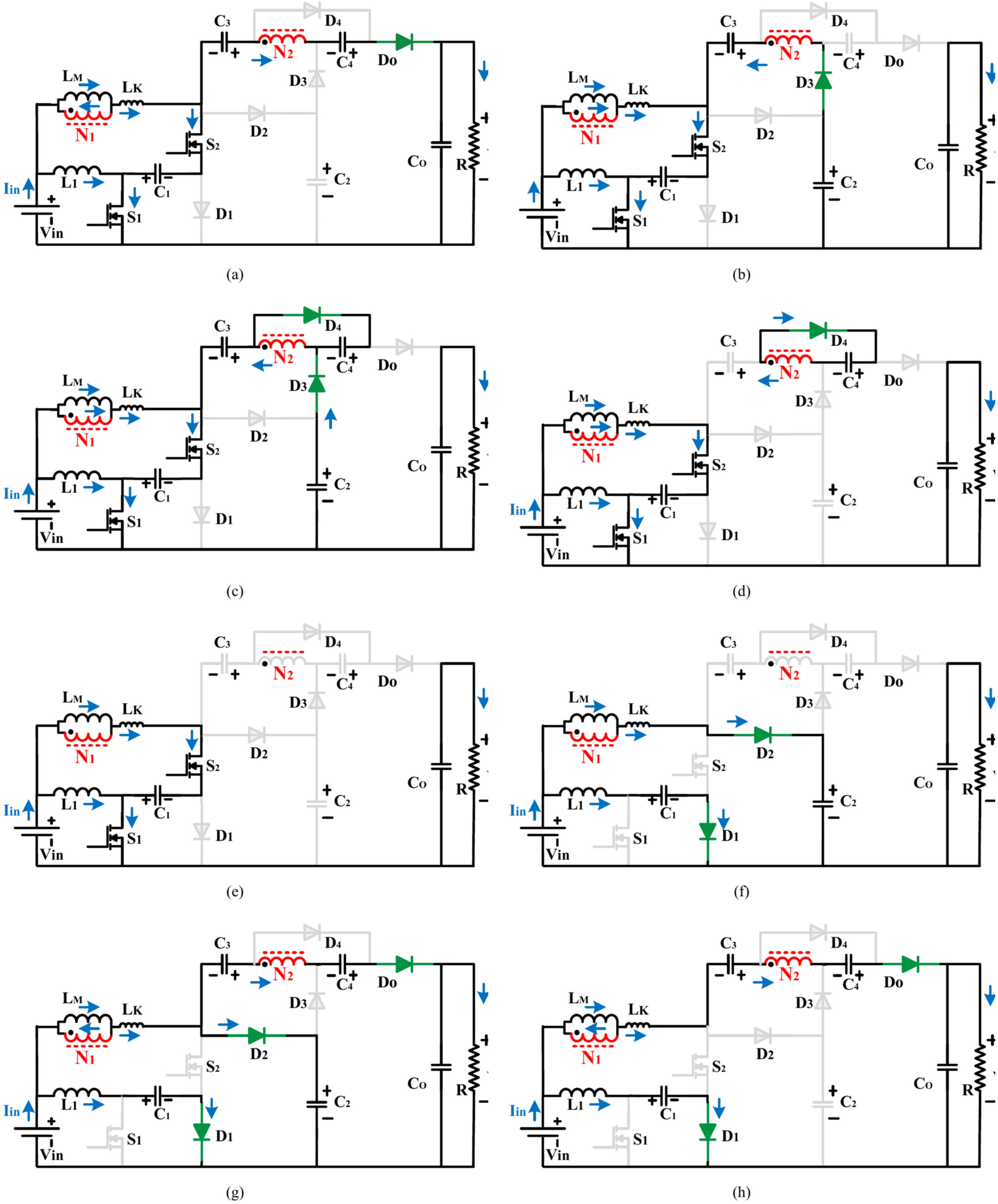


Fig. 2. Key waveforms of the proposed converter in CCM.



(a) (b) (c) (d) (e) (f) (g) (h)

Fig. 3. Equivalent circuits of the proposed converter.

The leakage inductor controls the slopes of the currents of D_3 and D_4 as below:

$$\frac{d\left(i_{D3}+i_{D4}\right)}{dt}=\frac{V_{C3}-nV_{in}-\left(n+1\right)V_{C1}-V_{C2}}{n^2L_K} \tag{6}$$

This mode ends at t_3 when the passing current through D_3 reaches to zero and it turns OFF with ZCS performance.

Mode IV $[t_3\sim t_4]$: The equivalent circuit of this mode is shown in Fig. 3(d). The current of D_4 is decreasing during this mode to maintain the charge balance of C_4. The voltage across C_2 remains constant because there is no energy exchange. This mode ends at t_4 when the current of D_4 reaches to zero and it turns OFF with ZCS performance.

$$i_{S1}=i_{L1}+i_{LM}+ni_{D4} \tag{7}$$

$$i_{S2}=i_{LM}+ni_{D4} \tag{8}$$

$$\frac{di_{D4}}{dt}=\frac{V_{C4}-n\left(V_{in}+V_{C1}\right)}{n^2L_K} \tag{9}$$

Mode V $[t_4\sim t_5]$: The equivalent circuit of this mode is shown in Fig. 3(e). All diodes ar OFF through this mode and the capacitor C1 continues discharging by the magnetizing inductor current.

$$i_{S1}=i_{L1}+i_{LM} \tag{10}$$

$$i_{S2}=i_{LM} \tag{11}$$

Mode VI $[t_5\sim t_6]$: The equivalent circuit of this mode is shown in Fig. 3(f). At time t_5, the power MOSFETs are turned OFF. Diodes D_1 and D_2 are turned ON to handle the currents of the L_1 and L_M which avoids high voltage spikes across the switches and also clamp the voltages of the power switches at $V_{S1}=V_{C1}$ and $V_{S2}=V_{C2}$. The voltages across L_1 and L_M are $V_{in}-V_{C1}$ and $V_{in}-V_{C2}$, respectively and as a result they are discharging, during this mode. Capacitors C_1 and C_2 start charging at the beginning of this mode and the output load is still supplied by C_O. This mode ends at t_6 when the voltage of C_2 is sufficiently high to forward bias diode D_O.

Mode VII $[t_6\sim t_7]$: The equivalent circuit of this mode is shown in Fig. 3(g). Part of the stored energy in the magnetizing inductor is transferring to the load via transformer effect through capacitors C_3, C_4 and diode D_O. which results in discharging of the mentioned capacitors. During this time interval, the passing currents of D_2 and D_O are decreasing and increasing, as well and are controlled by the leakage inductor. This mode ends at t_7 when the current passing D_2 reaches to zero and it turns OFF with ZCS.

$$\frac{di_{DO}}{dt}=\frac{-1}{n+1}\times\frac{di_{D2}}{dt}=\frac{\left(n+1\right)V_{C2}+V_{C3}+V_{C4}-nV_{in}-V_O}{n^2L_K} \tag{12}$$

Mode VIII $[t_7\sim t_8]$: The equivalent circuit of this mode is shown in Fig. 3(h). During this mode, the stored energy of the magnetizing inductor is still transferring to the load and the stored energy of L_1 is charging the capacitor C_1. This mode ends at t8 when the gate pulses of the power switches arrive and the next switching cycle starts.

B. DCM operation

Referring to mode VIII in Fig. 3(h), if the energy of the magnetizing inductor is decreased to zero, the DCM is achieved. Figure 4 shows the key waveforms and the equivalent circuit of the proposed converter for DCM in which for simplicity only the inductors' current waveforms along with the i_{DO} are provided and short duration modes aren't considered.

Steady-state analysis

To simplify the analysis, the leakage inductor effect is neglected. Moreover, the capacitors' voltages are considered constant.

A. CCM operation

Durin ON-state of the switches (mode III), the following equation are valid:

$$V_{L1}^{III}=V_{in} \tag{13}$$

$$V_{LM}^{III}=V_{in}+V_{C1} \tag{14}$$

$$V_{C3}=V_{C1}+V_{C2}+V_{C4} \tag{15}$$

$$V_{C4}=n\left(V_{in}+V_{C1}\right) \tag{16}$$

While the switches are OFF (mode VII), we have:

$$V_{L1}^{VII}=V_{in}-V_{C1} \tag{17}$$

$$V_{LM}^{VII}=V_{in}-V_{C2} \tag{18}$$

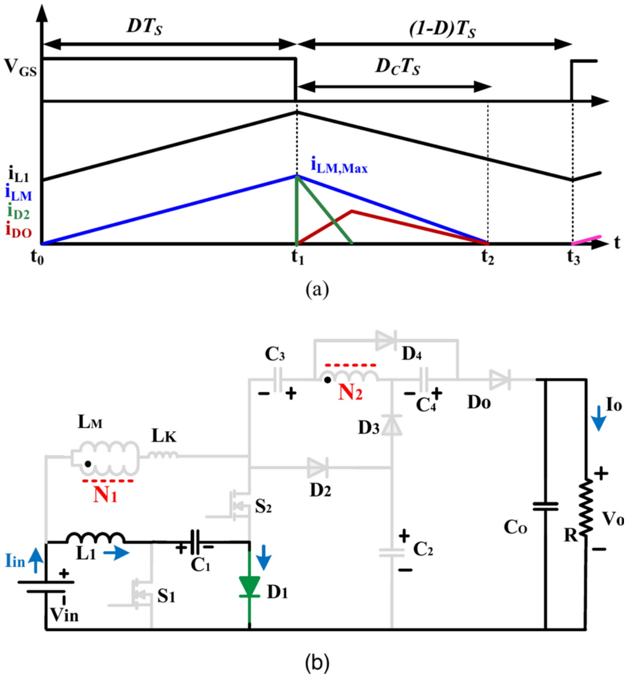


Fig. 4. DCM operation, (**a**) key waveforms, (**b**) equivalent circuit.

$$V_O = (n+1)\,V_{C2} + V_{C3} + V_{C4} - nV_{in} \tag{19}$$

By applying the volt-second balance principle to L_1 and L_M the voltages of V_{C1} and V_{C2} are obtained to be:

$$V_{C1} = \frac{1}{1-D}V_{in} \tag{20}$$

$$V_{C2} = \frac{1}{(1-D)^2}V_{in} \tag{21}$$

From (15) and (16), we have:

$$V_{C3} = \frac{(2-D)\,[1+n(1-D)]}{1-D}V_{in} \tag{22}$$

$$V_{C4} = n\left(\frac{2-D}{1-D}\right)V_{in} \tag{23}$$

Finally, by substituting of (21)-(23) into (19), the voltage gain of the proposed converter at CCM is expressed as:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1+(2-D)\,[1+n\,(2-D)]}{(1-D)^2} \tag{24}$$

It is seen from (24), that the voltage gain is considerably increased by the duty cycle and the turns ratio of the CI.

The voltage stresses across the power switches are obtained as

$$V_{S1} = V_{C1} = \frac{1}{1-D}V_{in} = \frac{1-D}{1+(2-D)\,[1+n\,(2-D)]}V_O \tag{25}$$

$$V_{S2} = V_{C2} = \frac{1}{(1-D)^2}V_{in} = \frac{1}{1+(2-D)\,[1+n\,(2-D)]}V_O \tag{26}$$

It is clear from (25) and (26) that the voltage stresses across the switches are successfully decreased by increasing of the turns' ratio of the CI. As a result, switches with low ON-state resistances could be selected to improve performance operation of the converter.

The imposed voltages across the diodes are obtained as

$$V_{D1} = V_{C1} = \frac{1-D}{1+(2-D)\,[1+n\,(2-D)]}V_O \tag{27}$$

$$V_{D2} = V_{C1} + V_{C2} = \frac{2 - D}{1 + (2 - D)\left[1 + n\left(2 - D\right)\right]}V_O \tag{28}$$

$$V_{D3} = V_{DO} = V_O - V_{C2} - V_{C4} = \frac{(2 - D)\left[1 + nD\left(2 - D\right)\right]}{1 + (2 - D)\left[1 + n\left(2 - D\right)\right]}V_O \tag{29}$$

$$V_{D4} = V_{C1} = \frac{n\left(2 - D\right)}{1 + (2 - D)\left[1 + n\left(2 - D\right)\right]}V_O \tag{30}$$

Along with the voltage stresses analysis, the current stresses analysis of the semiconductors and other components are necessary for design considerations and also efficiency estimation. Due to the ampere-second balance principle, the average value of the passing current through the capacitors is zero. As a result, the average currents of the diodes over a switching cycle are obtained as:

$$I_{D2,Ave} = I_{D3,Ave} = I_{D4,Ave} = I_{DO,Ave} = I_O \tag{31}$$

From the equivalent circuit of Fig. 3(g), the following equation can be obtained:

$$I_{LM} = \overline{i_{D2}} + (n+1)\,\overline{i_{DO}} \tag{32}$$

where, I_{LM} is the average current of the magnetizing inductor and $\overline{i_{D2}}$ and $\overline{i_{DO}}$ are the small ripple approximated (SRA) values of the passing current of diodes D_2 and D_O. The SRA values are obtained $I_O/1 - D$. Therefore, I_{LM} is derived as

$$I_{LM} = \frac{n+2}{1-D}I_O \tag{33}$$

By writing the KCL law at the bottom line of the converter in Fig. 1 and averaging the equation, the average value of current of L_1 is obtained as

$$I_{L1} = \left(M_{CCM} - \frac{n+3-D}{1-D}\right)I_O \tag{34}$$

Diode D_1, passes i_{L1} for about $(1-D)\,T_S$. As a result, the average current passing through this diode is given by

$$I_{D1} = \left(M_{CCM} - \frac{n+3-D}{1-D}\right)(1-D)\,I_O \tag{35}$$

The maximum and RMS current stresses of the components are summarized as

$$I_{D1,Max} = i_{L1,Max} = I_{L1} + \frac{DV_{in}}{2L_1 f_S} \tag{36}$$

$$I_{D2,Max} = i_{LM,Max} = I_{LM} + \frac{D\left(V_{in} + V_{C1}\right)}{2L_M f_S} \tag{37}$$

$$I_{D3,Max} = I_{D4,Max} = \frac{4}{D}I_O \tag{38}$$

$$I_{DO,Max} = \frac{i_{LM}(t_7)}{n+1} \tag{39}$$

$$I_{S1,Max} = I_{LM} + (n+1)\,I_{D3,Max} + I_{L1} \tag{40}$$

$$I_{S2,Max} = I_{LM} + (n+1)\,I_{D3,Max} \tag{41}$$

$$I_{S1,(t5)} = i_{L1,Max} + i_{LM,Max} \tag{42}$$

$$I_{S2,(t5)} = i_{LM,Max} \tag{43}$$

$$I_{D1,RMS} = I_{L1}\sqrt{1-D} \tag{44}$$

$$I_{D2,RMS} = \sqrt{\frac{2i_{LM,Max}I_O}{3}} \tag{45}$$

$$I_{D3,RMS} = I_{D4,RMS} = 4I_O\sqrt{\frac{1}{6D}} \tag{46}$$

$$I_{DO,RMS} = I_O\sqrt{\frac{1}{1-D}} \tag{47}$$

$$I_{C1,RMS} = \sqrt{I_{D1,RMS}^2 + I_{S2,RMS}^2} \tag{48}$$

$$I_{C2,RMS} = \sqrt{I_{D2,RMS}^2 + I_{D3,RMS}^2} \tag{49}$$

$$I_{C3,RMS} = \sqrt{I_{D3,RMS}^2 + I_{DO,RMS}^2} \tag{50}$$

$$I_{C4,RMS} = \sqrt{I_{D4,RMS}^2 + I_{DO,RMS}^2} \tag{51}$$

$$I_{CO,RMS} = \sqrt{I_{DO,RMS}^2 - I_O^2} \tag{52}$$

$$I_{LK,RMS}^{N2} = \sqrt{I_{D3,RMS}^2 + I_{D4,RMS}^2 + I_{DO,RMS}^2} \tag{53}$$

$$I_{LK,RMS}^{N1} = \sqrt{I_{LM}^2 + 2nI_{LM}I_O + \left(nI_{LK,RMS}^{N2}\right)^2} \tag{54}$$

$$i_{S1,RMS} = \sqrt{I_{L1}^2 + i_{C1,RMS}^2} \tag{55}$$

$$i_{S2,RMS} = \left(I_{LM} + \frac{2N+1}{D} I_o\right)\sqrt{D} \tag{56}$$

B. DCM operation

The equations of (13)-(16), (17)-(20) and (23) are also true for DCM operation. By applying the volta second-principle for L_M, the following equation is derived

$$V_{C2} = \frac{(D + D_C)\,V_{in} + DV_{C1}}{D_C} \tag{57}$$

By substituting (20), (23) and (56) in to the (15), we have

$$V_{C3} = \frac{n\,(2-D)+1}{1-D} + \frac{(D + D_C)\,V_{in} + DV_{C1}}{D_C} \tag{58}$$

Substituting of (56) and (57) in to the (19) yields

$$V_O = \frac{(n+2)\,[(D + D_C)\,V_{in} + DV_{C1}]}{D_C} + \frac{n\,(3-D)+1}{1-D} V_{in} \tag{59}$$

The peak value of the magnetizing inductor current in DCM operation can be obtained as below

$$I_{LM,Max} = \frac{D\,(2-D)}{(1-D)\,L_M f_S} V_{in} \tag{60}$$

On the other hand, the SRA of the passing current through D_2, D_O and L_M are obtained as

$$\overline{i_{D2}} = \overline{i_{DO}} = \frac{I_O}{D_C} \tag{61}$$

$$\overline{i_{LM}} = \frac{1}{2} I_{LM,Max} \tag{62}$$

Moreover, similar to derivation process of (33) in CCM; using (57), the following equation is proved in DCM:

$$\overline{i_{LM}} = \frac{n+2}{D_C} I_O \tag{63}$$

From (58), (60) and (62), D_C is derived as

$$D_C = \frac{2\,(n+2)\,(1-D)}{D(2-D)} \tau_{LM} M_{DCM} \tag{64}$$

where $\tau_{LM} = L_M f_S / R_O$ and M_{DCM} is the voltage gain of the proposed converter in DCM.

By substituting (62) in to the (57) and some manipulation, the voltage gain of the proposed converter in DCM is obtained as below

$$M_{DCM} = \frac{V_O}{V_{in}} = \frac{\alpha_1 \tau_{LM} (\alpha_2 + n + 2) + \sqrt{[\alpha_1 \tau_{LM} (\alpha_2 + n + 2)]^2 + 4\alpha_1 \alpha_3}}{2\alpha_1 \tau_{LM}} \tag{65}$$

where,

$$\alpha_1 = \frac{2(n+2)(1-D)}{D(2-D)}; \ \alpha_2 = \frac{n(3-D)+1}{1-D}; \ \alpha_3 = D(n+2)\left(\frac{2-D}{1-D}\right)$$

C. BCM operation

In the BCM mode, the voltage gains of M_{CCM} and M_{DCM} are equal and the average value of the magnetizing inductor current given in (33) is equal to half of its maximum value that is written as

$$\frac{1}{2} I_{LM,Max} = I_{LM} = \frac{n+2}{1-D} I_O \tag{66}$$

By substituting of (58) in to the (65), the boundary frequency constant (τ_{LMB}) is derived as

$$\tau_{LMB} = \frac{L_{MB} f_S}{R_O} = \frac{D(2-D)}{2(n+2) M_{CCM}} \tag{67}$$

Figure 5 shows τ_{LMB} versus D. For $\tau_{LMB} < \tau$, the proposed converter operates in CCM while $\tau_{LMB} > \tau$ results in DCM.

Comparison discussion

The advantages of the proposed converter are highlighted by a comprehensive comparison with recently published similar topologies given in Table 1. Figure 6 shows the comparison of voltage gain and voltage stresses of semiconductors. $n_{21} = n_{31} = 0.5$ is considered for the converters with three-winding CI and to have a fair comparison, $n = n_{21} + n_{31} = 1$ is selected for the topologies with two-winding CI.

Figure 6(a) depicts the comparison of the voltage gain per number of the components. It is seen that the proposed converter has the highest value of all and it reveals that the components are effectively participating in voltage gain extension. Figure 6(b) shows the comparison of the voltage stresses of the power MOSFETs. It is seen that in the proposed converter, the imposed voltage stress is the lowest facilitating the implementation of low voltage rated MOSFETs. Figure 6(c) illustrates the comparison of the normalized voltage stresses across diodes. In each of the competitors a diode with the highest voltage stress has been selected and provided for comparison. It is seen that that the mentioned diode in the proposed converter tolerates relatively low voltage stress when compared to other ones.

S = Switch, **D** = Diode, **C** = Capacitor, **CI** = Coupled-Inductor, **L** = Inductor, **T** = Total Device, **C.I.C.R** = Continuous Input Current Ripple, **C.G** = Common Ground.

Small singal modeling of the proposed converter

This section provides the small signal derivation along with the low-frequency behavior of the suggested converter. To simplify the modeling process, the state-space averaging method is considered[40]. According to th structure of the proposed circuit, the state variable vector is given as:

$$x(t) = [i_{L1} i_{LM} v_{C1} v_{C2} v_{C3} v_{C4} v_{Co}] \tag{68}$$

To extract the state equations of the proposed converter in main modes including 3, and 7, it is necessary to consider the parasitic resistance r_{c1} , and r_{c2} in series with the capacitors C_1, and C_2 respectivily. It should be noted that consideration of all parasitic elements leads to more complicated to obtain the state equations. Regarding the proposed converter structure, the state equations of the proposed converter are obtained as follows:

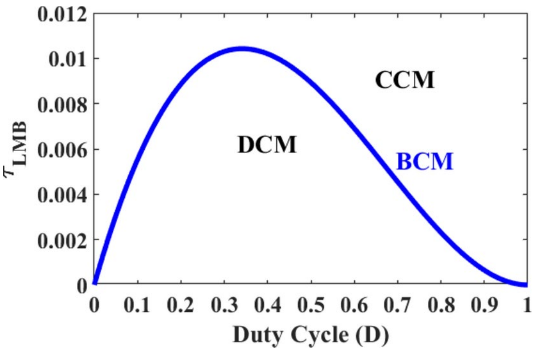


Fig. 5. Boundary curve between CCM and DCM.

Converter Topology	No. of Components	Voltage Gain	C.I.C.R	Voltage Stress on Main Power Switch	Maximum Voltage Stress on Diodes	C.G
	S/D/C/CI + L/T					
[5]	1/7/5/0 + 3/16	$\frac{4}{(1-D)^2}$	No	$\frac{V_o}{2}$	$\frac{V_o}{2}$	Yes
[9]	1/5/6/0 + 4/16	$\frac{1+2\mathrm{D}-2D^2}{(1-D)^2}$	Yes	$\frac{V_o}{1+2\mathrm{D}-2D^2}$	$\frac{V_o}{1+2\mathrm{D}-2D^2}$	Yes
[14]	$1/6/5/1^{2w}+1/14$	$\frac{1+n-\mathrm{n}D^2}{(1-D)^2}$	No	$\frac{V_o}{1+n-\mathrm{n}D^2}$	$\frac{(1-D)V_o}{1+n-\mathrm{n}D^2}$	Yes
[16]	$1/5/4/1^{2w}+1/12$	$\frac{2+n}{(1-D)^2}$	Yes	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	Yes
[17]	$1/5/4/1^{2w}+1/12$	$\frac{2+n}{(1-D)^2}$	Yes	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	Yes
[18]	$1/6/5/1^{2w}+1/14$	$\frac{2+n(2-D)}{(1-D)^2}$	Yes	$\frac{V_o}{2+n(2-D)}$	$\frac{(1+n)V_o}{2+n(2-D)}$	Yes
[21]	$2/1/2/2^{2w}+0/9$	$\frac{(2-\mathrm{D})(n_{21}+n_{31}(1-\mathrm{D}))+(1-\mathrm{D})}{(1-D)^2}$	No	$\frac{DV_o}{(2-\mathrm{D})(n_{21}+n_{31}(1-\mathrm{D}))+(1-\mathrm{D})}$	$\frac{(n_{31}+n_{21}(1-\mathrm{D}))V_o}{(2-\mathrm{D})(n_{21}+n_{31}(1-\mathrm{D}))+(1-\mathrm{D})}$	Yes
[22]	$1/7/5/1^{2w}+2/16$	$\frac{1+n}{(1-D)^2}$	Yes	$\frac{V_o}{2}$	$\frac{(1+nD)V_o}{1+n}$	Yes
[23]	$1/5/4/1^{3w}+1/12$	$\frac{1+n_2+n_3\mathrm{D}}{(1-D)^2}$	Yes	$\frac{V_o}{1+n_2+n_3\mathrm{D}}$	$\frac{(1+n_2)V_o}{1+n_2+n_3\mathrm{D}}$	Yes
[24]	$1/5/4/1^{3w}+1/12$	$\frac{n_{21}+n_{31}(1-D)+2-D}{(1-D)^2}$	Yes	$\frac{V_o}{n_{21}+n_{31}(1-D)+2-D}$	$\frac{(n_{21}+2-D)V_o}{n_{21}+n_{31}(1-D)+2-D}$	Yes
[25]	$2/5/5/1^{2w}+1/14$	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	Yes	$\frac{(1-D)V_o}{3+2n-D(3+n-D)}$	$\frac{n(2-D)V_o}{3+2n-D(3+n-D)}$	Yes
[26]	$2/4/5/1^{4w}+1/13$	$\frac{1+n_{21}+n_{31}}{(1-D)^2}$	Yes	$\frac{V_o}{1+n_{21}+n_{31}}$	$\frac{(n_{21}+n_{31})V_o}{1+n_{21}+n_{31}}$	Yes
[27]	$1/4/3/1^{3w}+1/10$	$\frac{(2+n_{21}+n_{31})-(n_{31}+1)D}{(1-D)^2}$	Yes	$\frac{V_o}{(2+n_{21}+n_{31})-(n_{31}+1)D}$	$\frac{(1+n_{21}+n_{31})V_o}{(2+n_{21}+n_{31})-(n_{31}+1)D}$	No
[28]	$1/3/4/1^{3w}+1/10$	$\frac{2+n_{21}-n_{31}}{(1-n_{31})(1-D)}$	No	$\frac{(1-n_{31})V_o}{2+n_{21}-n_{31}}$	$\frac{(1+n_{21})(1-n_{31})V_o}{2+n_{21}-n_{31}}$	No
[29]	$1/6/5/1^{3w}+1/14$	$\frac{2+n_{21}+n_{31}-n_{31}D}{(1-D)^2}$	Yes	$\frac{V_o}{2+n_{21}+n_{31}-n_{31}D}$	$\frac{(1+n_{21}+n_{31})V_o}{2+n_{21}+n_{31}-n_{31}D}$	No
[37]	$1/4/5/1^{2w}+1/12$	$\frac{1+\mathrm{D}+n_{21}-n_{31}}{(1-n_{31})(1-D)}$	Yes	$\frac{(1-n_{31})V_o}{1+\mathrm{D}+n_{21}-n_{31}}$	$\frac{V_o}{1+\mathrm{D}+n_{21}-n_{31}}$	Yes
[38]	$1/4/5/1^{2w}+1/12$	$\frac{1+2n_{31}-\mathrm{D}(n_{21}+n_{31}-1)}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{1+2n_{31}-\mathrm{D}(n_{21}+n_{31}-1)}$	$\frac{(1+n_{31})V_o}{1+2n_{31}-\mathrm{D}(n_{21}+n_{31}-1)}$	Yes
Proposed Converter	$2/5/5/1^{3w}+1/14$	$\frac{1+(2-D)[1+n(2-D)]}{(1-D)^2}$	Yes	$\frac{(1-D)V_o}{1+(2-D)[1+n(2-D)]}$	$\frac{(2-D)(1+nD(2-D))]V_o}{1+(2-D)[1+n(2-D)]}$	Yes

Table 1. Performance comparison of the proposed converter with other counterparts.

According to Fig. 3 (c), the state equations of mode 3 are expressed as:

$$L_1\frac{di_{L1}}{dt}=V_{in} \tag{69}$$

$$L_M\frac{di_{LM}}{dt}=X_0V_{C4} \tag{70}$$

$$C_1\frac{dV_{c1}}{dt}=-X_1V_{in}+X_1X_0V_{C4}-X_1V_{C1} \tag{71}$$

$$C_2\frac{dV_{c2}}{dt}=X_2V_{in}+X_2V_{C3}-X_2V_{C2}-X_2X_3V_{C4} \tag{72}$$

$$C_3\frac{dV_{c3}}{dt}=-X_2V_{in}-X_2V_{C3}+X_2V_{C2}+X_2X_3V_{C4} \tag{73}$$

$$C_4\frac{dV_{C4}}{dt}=(X_2X_3+X_0X_1)V_{in}+X_0X_1V_{C1}-X_2X_3V_{C2}+X_2X_3V_{C3}-(X_2{X_3}^2+X_1{X_0}^2)V_{C4}-X_0i_{LM} \tag{74}$$

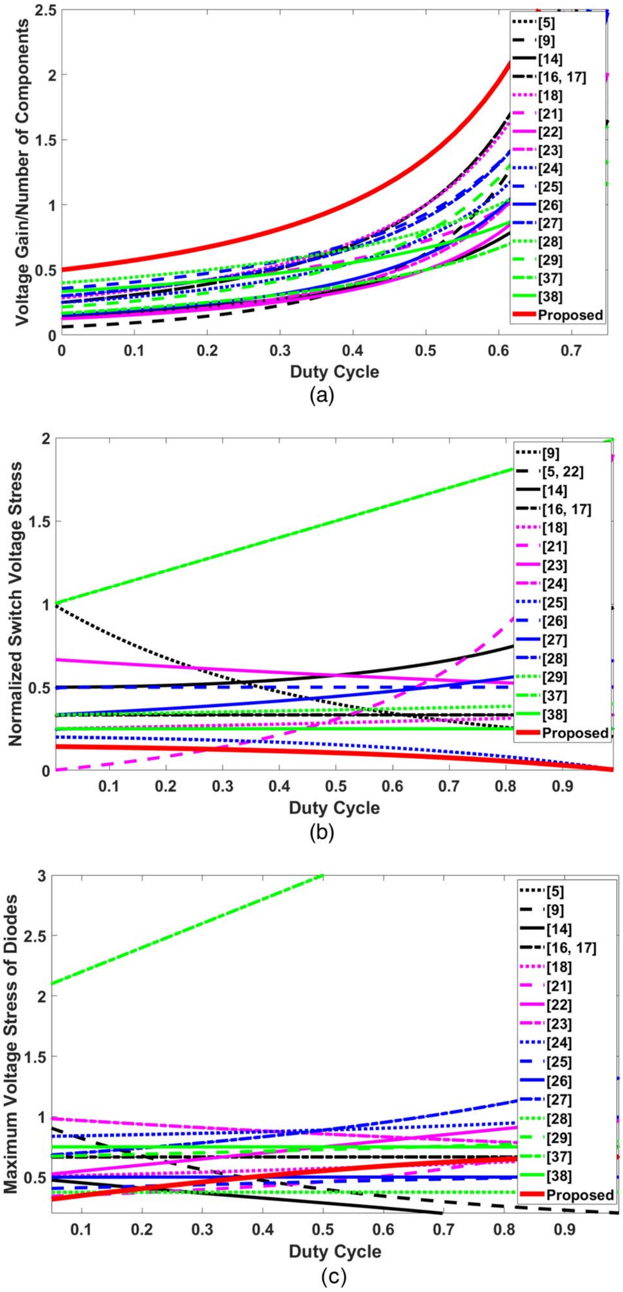
$$C_o\frac{dV_{co}}{dt}=-\frac{V_{Co}}{R} \tag{75}$$

The state equations of mode 7 based on Fig. (g), are given as:

$$L_1\frac{di_{L1}}{dt}=V_{in}-V_{C1}-r_{C1}i_{L1} \tag{76}$$

$$L_M\frac{di_{LM}}{dt}=X_4V_{in}+X_4V_{C3}+X_4V_{C4}-X_4V_{Co} \tag{77}$$

$$C_1\frac{dV_{c1}}{dt}=i_{L1} \tag{78}$$



(a)

(b)

(c)

Fig. 6. Performance comparison of the proposed converter, (**a**) voltage gain per number of the components, (**b**) normalized voltage stress across the power MOSFET, (**c**) normalized maximum voltage stresses across the diodes.

$$C_2\frac{dV_{c2}}{dt} = X_2X_5V_{in} - X_2V_{C2} - X_2X_4V_{C3} - X_2X_4V_{C4} + X_2X_4V_{Co} \tag{79}$$

$$C_3\frac{dV_{c3}}{dt} = X_2X_4X_5V_{in} - X_2X_4V_{C2} - {X_4}^2X_2V_{C3} - {X_4}^2X_2V_{C4} + {X_4}^2X_2V_{Co} - X_4i_{Lm} \tag{80}$$

$$C_4\frac{dV_{C4}}{dt} = X_2X_4X_5V_{in} - X_2X_4V_{C2} - {X_4}^2X_2V_{C3} - {X_4}^2X_2V_{C4} + {X_4}^2X_2V_{Co} - X_4i_{Lm} \tag{81}$$

$$C_o\frac{dV_{co}}{dt} = -X_2X_4X_5V_{in} + X_2X_4V_{C2} + {X_4}^2X_2V_{C3} + {X_4}^2X_2V_{C4} - {X_4}^2X_2V_{Co} + X_4i_{Lm} - \frac{V_{Co}}{R} \tag{82}$$

where X_1-X_6 are defined as follows:

$$X_0 = \frac{1}{n} \tag{83}$$

$$X_1 = \frac{1}{r_{c1}} \tag{84}$$

$$X_2 = \frac{1}{r_{c2}} \tag{85}$$

$$X_3 = 1 + \frac{1}{n} \tag{86}$$

$$X_4 = \frac{1}{1+n} \tag{87}$$

$$X_5 = \frac{n}{1+n} \tag{88}$$

By Considering the weighting factors including *d*, and (*1-d*) for the operational modes of the introduced circiot, the averaged model is achieved as:

$$\begin{cases} \widehat{\dot{x}} = A\hat{x} + B\hat{u} \\ \widehat{y} = C\hat{x} + D\hat{u} \end{cases} \tag{89}$$

$$\begin{cases} A = dA_1 + (1-D)A_2 \\ B = dB_1 + (1-D)B_2 \\ C = dC_1 + (1-D)C_2 \\ D = dD_1 + (1-D)D_2 \end{cases} \tag{90}$$

Here A_i, B_i, C_i and D_i are the state matrices, *y* are the output voltage, *x* denotes the averaged value of the state variables and also *u* is the input source. To derive the small-signal model of the system, the small ac perturbations are superimposed to the variable states as follows:

$$\begin{cases} d = D + \hat{d} \\ u = U + \hat{u} \\ x = X + \hat{x} \end{cases} \tag{91}$$

Here, lower case variables denote the small value of the parameters and capital variables are the steady-state values. By substituting (89) into (87), and neglecting steady-state terms, the transfer functions output-to-input (G_{vov}) and the output-to-duty cycle (G_{vod}) of the converter are obtained as:

$$Gvov = \frac{vo}{vi} = \left.\frac{\hat{y}(s)}{\hat{u}(s)}\right|_{\hat{d}=0} = C(SI - A)^{-1}B + D \tag{92}$$

The control-to-output voltage transfer function G_{vod} is also obtained as:

$$G_{vod} = \frac{v_o}{d} = C(SI-A)^{-1}\left[(A_1 - A_2)\,X - (B_1 - B_2)\,U\right] + (C_1 - C_2)\,X + + (D_1 - D_2)\,U \tag{93}$$

Bode plot diagrams of the transfer functions G_{vov} and G_{vod} obtained using this method are presented in Fig. 7 and Fig. 8 for a constant output load R = 800 Ω, V_{out} = 400 V, *n* = 0.6, V_{in} = 25V, M = 16, and D = 0.51. From these figures, the proposed converter is stable with non-minimum phase behaviors. Also, Fig. 9 shows the pole and zero placement map for the transfer function G_{vod} . It should be noted that the non-minimum phase behavior is one of the most prominent behaviour of the high-gain DC-DC converters, which is due to the presence to the right half-plane zero/zeros of the control—output transfer function. Based on the simulation parameters used in the sample prototype , the control-to-output (G_{vod}) transfer function in is obtained as:

$$G_{vod} = \frac{-10192. * (\mathrm{s} + 1.137\mathrm{e}06). * (\mathrm{s} - 7.9\mathrm{e}04). * (\mathrm{s} + 4.81\mathrm{e}04). * (\mathrm{s} + 8206). * (\mathrm{s}^2 + 9.067. * \mathrm{s}\ + 8.992\mathrm{e}06)}{(\mathrm{s} + 1.157\mathrm{e}06). * (\mathrm{s} + 3.903\mathrm{e}04). * (\mathrm{s} + 1.396\mathrm{e}04). * (\mathrm{s}^2 + 273.4. * \mathrm{s}\ + 2.255\mathrm{e}05). * (\mathrm{s}^2 + 148.6. * \mathrm{s}\ + 1.729\mathrm{e}07)} \tag{93}$$

Experimental results

To prove the performance of the proposed converter a 200W prototype with 25 V-400 V voltage conversion is fabricated and tested in the laboratory. The specifications of the set-up are provided in Table 2 and the experimental results are shown in Fig. 10.

Figure 10(a) shows the gate-source pulse, input current and the output voltage. It is seen that the high output voltage of 400 V is obtained from 25 V input voltage at a duty cycle around 51%. Figure 10(b) demonstrate the passing currents through L_K and L_1 that are consistent with the analyzed key-waveforms of Fig. 2. Figure 10(c) and Fig. 10(d) illustrates the voltages and currents of the MOSFETs. S_1 and S_2 tolerate 56 V and 110 V, respectively. Moreover, ZCS performance is provided for S_2. Figure 10(e)–10(h) show the experimental results of the voltages

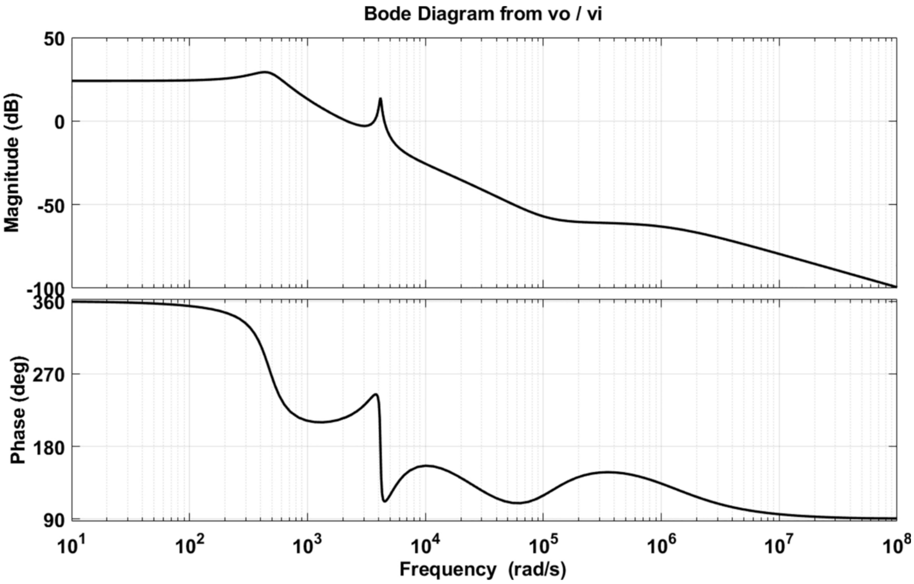


Fig. 7. Frequency response of the control-to-output transfer (Gvov) of the proposed topology.

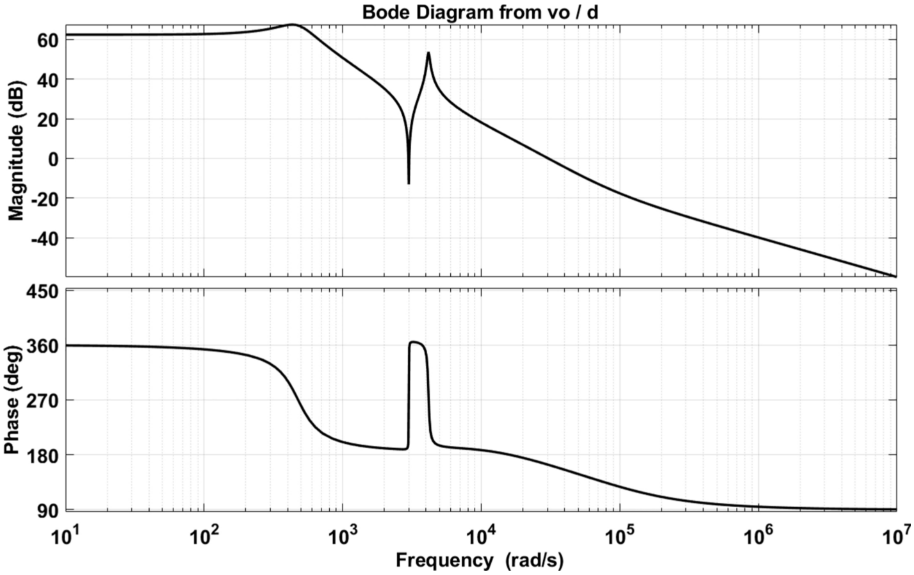


Fig. 8. Frequency response of the control-to-output transfer (Gvod) of the proposed topology.

and currents of the diodes. The imposed voltages across the diodes are about $V_{D1} = 56$ V, $V_{D2} = 155$ V, $V_{D3} = 230$ V, $V_{D4} = 100$ V, and $V_{Do} = 235$ V. The obtained values are consistent with the carried steady-state analysis in section III. Moreover, all diodes except D_1 are turned OFF with ZCS and the reverse recovery problem is alleviated.

Moreover, Fig. 10(i) presents the dynamic response of the proposed circuit under the output load variations. It is seen that when the output load change from $R_{Load1} = 800\ \Omega$ to $R_{Load2} = 1200\ \Omega$, the output voltage is regulated at 400V, successfully. To obtain these results, an additional load ($R_{L2} = 800\ \Omega$) has been placed in series with the converter load ($R_{L1} = 400\ \Omega$) in the sample prototype circuit. Then, under a very low switching frequency, this additional load ($R_{L2} = 400\ \Omega$) has been switched on in series continuously.

Figure 11 shows the measured efficiency of the proposed converter versus different values of the output power. The maximum efficiency is 96.2% at 160W and the full load efficiency is 95.9%. Also, Fig. 12 shows the losses distribution of the proposed converter at full load. The losses of the components are calculated as $P_{MOSFETs} = 0.7\,W$, $P_{Diodes} = 3.18\,W$, $P_{Magnetics} = 1.2\ W$ and $P_{Capacitors} = 0.13\,W$. The total power losses are about 5.22 W and the estimated efficiency is 97.46%.

The summary of the detailed power loss analysis of the introduced topology is presented in Table 3. Moreover, the simulation results of the magnetic field intensity and magnetic flux density inside the magnetic core EE

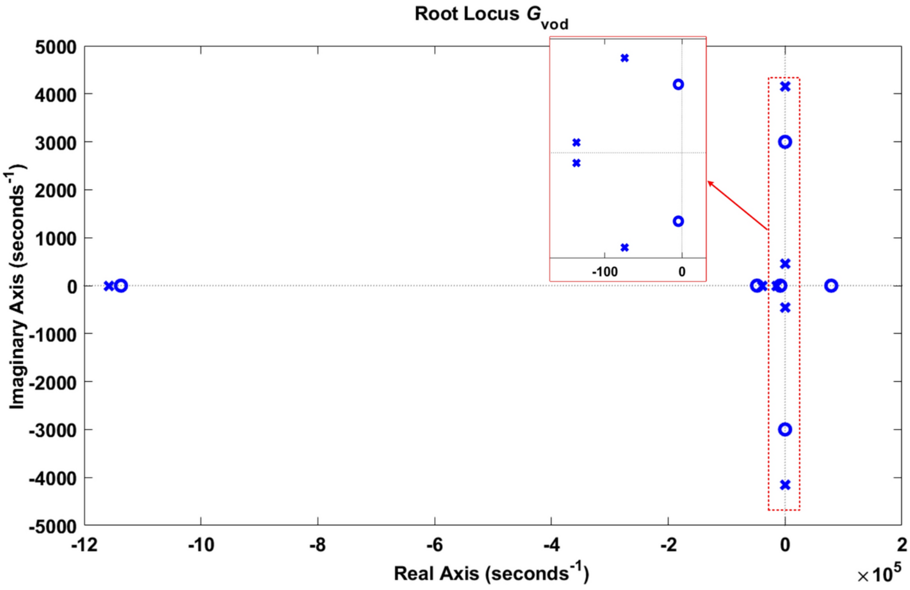


Fig. 9. Pole and zero map of the control-to-output transfer function.

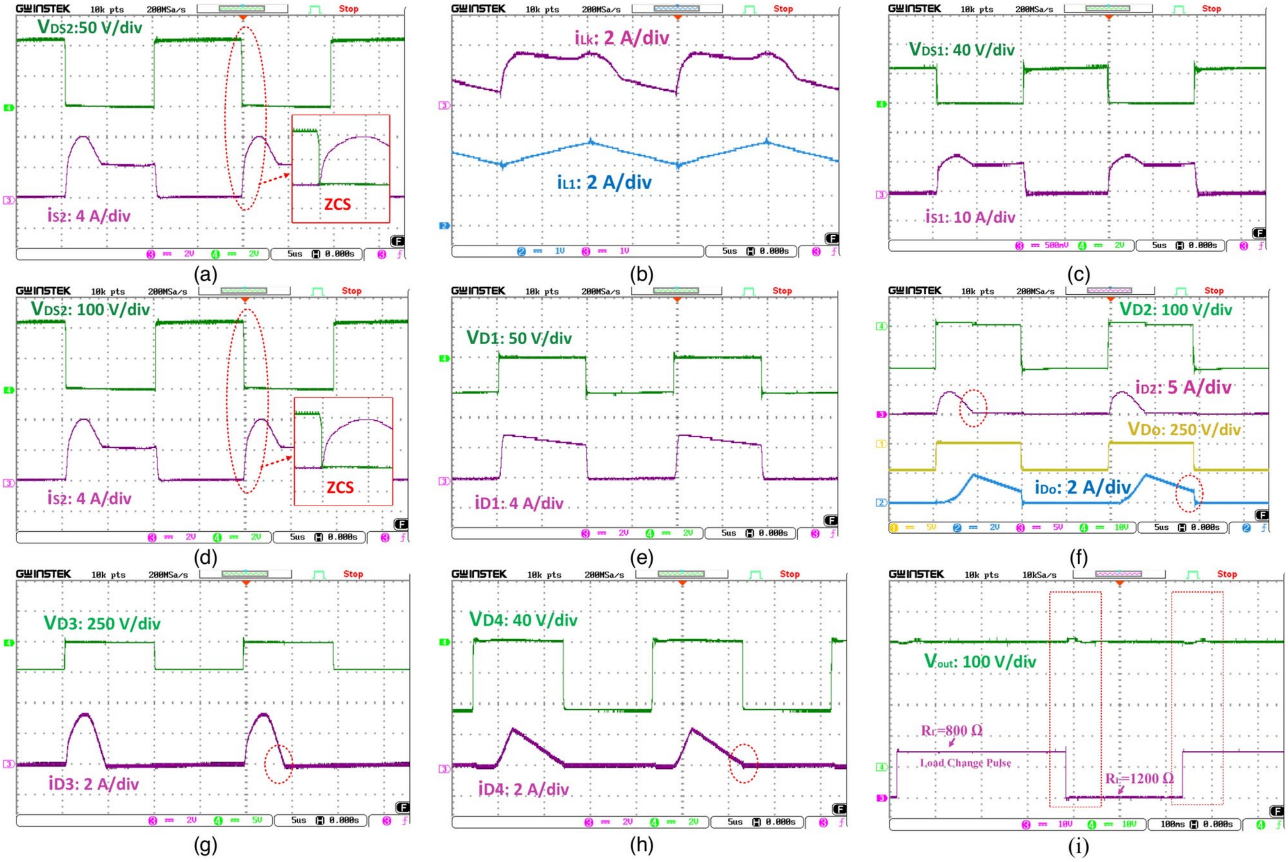
Parameter	Values
Output Power (P_{out})	200 W
Input Voltage (V_{in})	25 V
Output Voltage (V_o)	400 V
Switching Frequency (f_s)	50 kHz
Capacitor C_1	2*10 µF / 63 V
Capacitor C_2	10 µF / 250 V
Capacitor C_3	15 µF / 250 V
Capacitor C_4	100 µF / 200 V
Capacitor C_o	220 µF / 450 V
Power Switches S_1 and S_2	IPP076N15N5/ $R_{DS(on)}$=7.6 mΩ
Inductor L_1 / Core	160 µH / EE42/21/15
Magnetizing Inductor of the CL (L_m)	240 µH
Turns Ratios of the CI / Core	(1:0.65) / EE42/21/15
Diodes D_3, D_o	MUR440
Diodes D_2, D_4	MUR420
Diode D_1	MBR10100

Table 2. Key parameters of prototype setup.

42/21/15 used in the sample prototype of the proposed converter in FEMM software is provided is shown in Fig. 13. A Photo of the sample prototype of the introduced converter is presented in Fig. 14.

Conclusion

This paper presented a new non-isolated quadratic step-up DC-DC converter with a coupled inductor and low input current ripple for high step-up applications. Because of the current sharing between the input magnetic devices of this circuit along with the reduction of current and voltage tensions in the power switching devices, the power dissipations are alleviated. Furthermore, in this circuit, very high voltage gains can be offered under small turns ratios of the coupled-inductor, which decreases the wire parasitic resistances. Moreover, in this circuit, the leakage energy of the CI is recycled with the help of a simple clamp circuit which limits the voltage stresses on the circuit switches. In addition, the feasibility of the suggested topology is verified using the experimental results of a 200 *W*, 25 V/400 V /50 kHz sample prototype. The results obtained from the sample prototype along with theory indicate the low current and voltage stresses of the circuit elements and enough high efficiency; thus, the introduced topology can be an attractive selection for high-voltage gain DC/DC applications.



(a) (b) (c) (d) (e) (f) (g) (h) (i)

Fig. 10. Experimental results of the proposed converter.

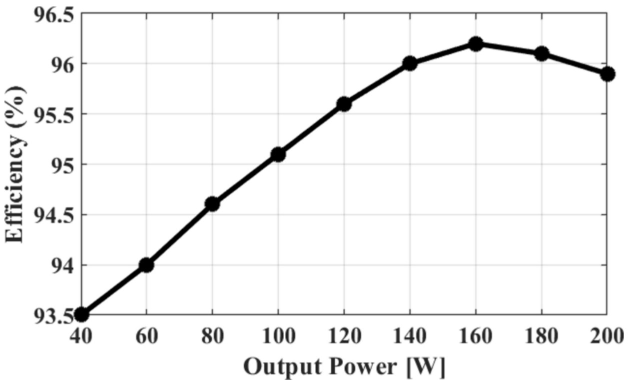


Fig. 11. Conversion efficiency of the proposed converter.

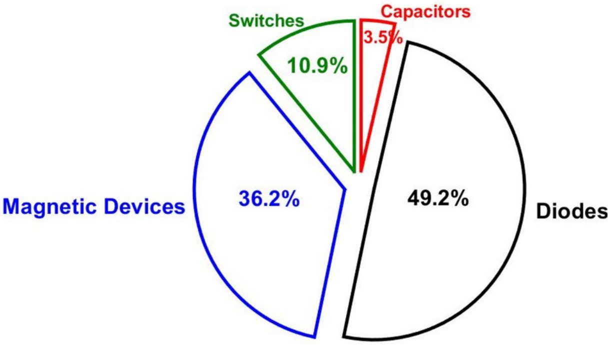


Fig. 12. Losses distribution of the proposed converter at full load.

Components	Power loss relations	Loss value (w)	Percent (%)
Inductor L_1	$P^{loss}_{ohmic}+P^{loss}_{core}$	0.59	10.3
CI loss	$P^{loss}_{ohmic}+P^{loss}_{core}$	1.47	25.8
MOSFET S_1	$\frac{1}{2T_s}\left(I_{switch(\text{off})}.V_{DS}.t_{off}\right)+\frac{1}{2T_s}\left(I_{switch(\text{on})}.V_{DS}.t_{oN}\right)+I^2_{S(RMS)}.R_{DS(on)}$	0.48	8.4
MOSFET S_2	$\frac{1}{2T_s}\left(I_{switch(\text{off})}.V_{DS}.t_{off}\right)+I^2_{S(RMS)}.R_{DS(on)}$	0.14	2.4
D_1	$V_F.I_{D(AVG)}$	1.3	22.8
D_2		0.37	6.5
D_3		0.42	7.3
D_4		0.35	6.1
D_o		0.41	7.2
C_1	$I^2_{C(RMS)}.ESR$	0.1	1.7
C_2		0.02	0.3
C_3		0.02	0.3
C_4		0.05	0.8
C_o		0.01	0.15

Table 3. The loss distributions of the proposed topology.

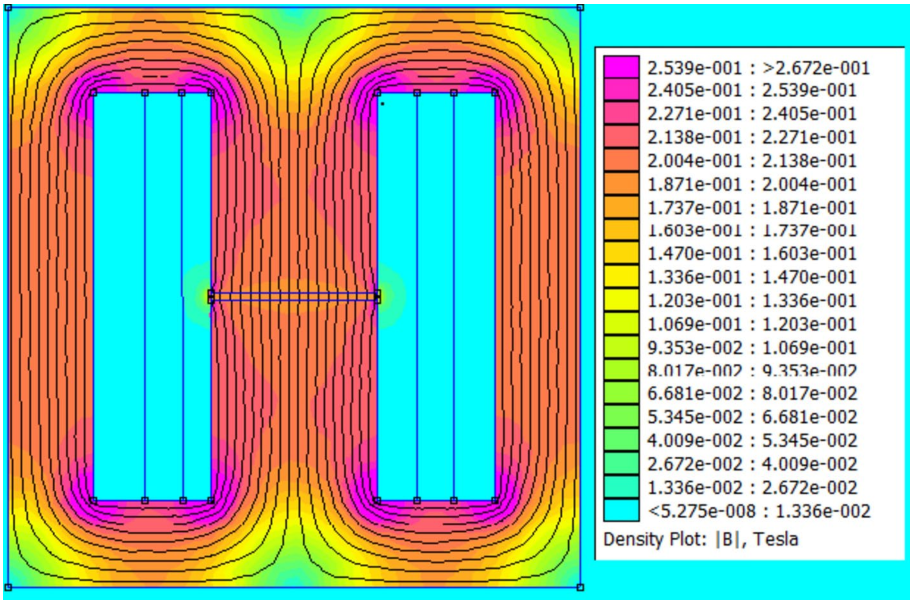


Fig. 13. The simulation results of the magnetic field intensity and magnetic flux density inside the magnetic core EE 42/21/15 used in the sample prototype of the proposed converter by FEMM software.

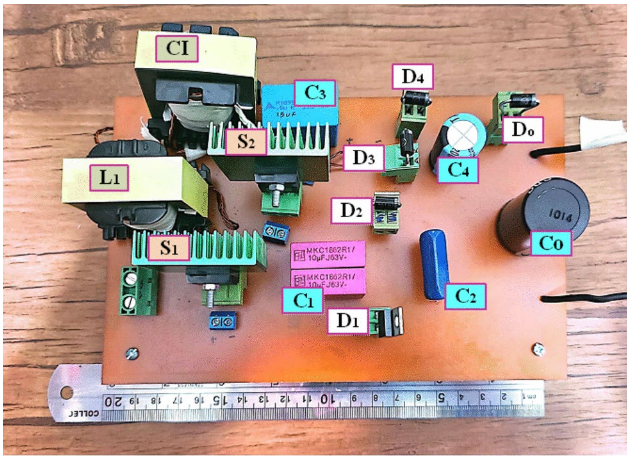


Fig. 14. Photograph of the proposed converter prototype.

Data availability

Data is provided within the manuscript.

Received: 7 November 2024; Accepted: 10 February 2025

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Author contributions

Sayed Jamal-Aldin Hosseini and Sara Hasanpour: Writing-original draft, methodology. Ghazanfar Shahgholian, Majid Moazzami, Amir Baktash: Editing, conceptualization and review.

Declaration

Competing interests

The authors declare no competing interests.

Additional information

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